Optimization of Photolithography Process for BiHEMT Gate Layer with High Critical Dimension Uniformity

Stephanie Y. Chang, Tom Brown, Randy Bryie, Rainier Lee

Skyworks Solutions, Inc., 2427 W. Hillcrest Drive, Newbury Park, CA 91320 [Stephanie.Chang@skyworksinc.com,](mailto:Stephanie.Chang@skyworksinc.com) (805) 871-6801

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Abstract

This paper describes a series of design of experiments (DOE) performed for optimizing BiHEMT gate layer's (GL) photolithography scheme to tighten statistical process control (SPC) of submicron critical dimension (CD) linewidths. Characterization studies investigated the influence of chemically amplified (CAMP) photoresist, wait time between exposure and post-exposure bake (PEB) steps, and the wafer's thermal history during PEB process on BiHEMT GL CD uniformity. Experimental findings allowed for fine-tuned photolithography recipes with exposure dose compensation to reduce intra-wafer CD variation. Implementation of additional process controls within the GL's fabrication process eliminated photolithography rework arising from poor CD uniformity and erratic trends.

INTRODUCTION

Widely used in cellular and wireless fidelity applications, BiHEMT devices allow for a reduction in module size and total chip costs while boosting design flexibility and functionality [1]. At Skyworks Solutions, BiHEMT devices were constructed from integrating finely tuned pseudomorphic high electron mobility transistor (pHEMT) with isolating InGaP/GaAs heterojunction bipolar transistor (HBT). To achieve high analog and radio frequency (RF) performance, it is crucial to address complex topology-related challenges that arise from the BiHEMT fabrication process as well as optimize photolithography and etch processes to welldefine the submicron pHEMT gate. To enable nextgeneration designs of power amplifiers with reduced footprint and circuit feature size, photolithography processes must be optimized to preserve the integrity of printed features onto photoresist [2]. Tightening the process margins for critical dimension (CD) uniformity while maintaining high yields in a high-volume manufacturing environment becomes necessary for repeatable high RF performance. In this study, the photolithography process that defines the pHEMT's gate layer (GL) was optimized to reduce intra-wafer, wafer-towafer, and lot-to-lot variation for submicron GL CD.

METHODOLOGY AND PROCESS CHARACTERIZATION

Various process parameters at different steps of the fabrication process' photolithography flow can impact the fidelity of the CD features. Inline verification that the patterns are correctly printed onto the photoresist is crucial before the pattern is etched into the wafer. To rule out the inconsistency of manual measurements, following the photoresist coat, exposure, post-exposure bake (PEB), and develop steps, an automated scanning electron microscope (SEM) job with optimized beam settings was used to measure the CD features in all exposure fields. To establish a correlation between the test and circuit structures, GL circuit features at the center and four corners of the stepper exposure field, as well as the center CD bar test structure on the process control monitor (PCM) coupon were measured as shown in Figure 1.

Fig. 1. (a) SEM image of the GL CD bar test structure and (b) location of GL features within an exposure field.

SOURCES OF CD VARIATION

High intra-wafer and wafer-to-wafer CD variation results in high photolithography rework rates. While CD variation can be attributed to various process and equipment related factors (e.g., stepper lithographic process parameters, mask pattern, diffraction limit of optics), this paper primarily examines the influence from the chemical amplification's reaction and wafer's thermal history during the PEB process.

Post-exposure Bake

For the BiHEMT GL process, chemically amplified (CAMP) negative tone photoresist was used to achieve the desirable photoresist profile and adequate adhesion to the underlying layer. Due to the photoresist's CAMP nature, multiple cross-linking reactions take place in the photoresist per absorbed photon. During the exposure process, photoresist is exposed with ultraviolet (UV) light; this activates the melamine cross-linker. PEB drives the thermal reaction that results in the decomposition and subsequent multiplication of photoacids in neighboring areas of the photoresist. Due to the cross-linking of the phenolic resin molecules to longer chains in the photoresist, the exposed regions become non-soluble in the developer.

To address the challenge of reducing variations in GL CD linewidth, a series of design of experiments (DOE) for the PEB process was performed on tightly controlled hot plates. PEB time and temperature were dialed-in to reduce the intrawafer CD linewidth variation. Figure 2 reveals a negative correlation between the PEB parameters (time, temperature) and GL CD distribution per wafer. Measurements of average CD bar and circuit structures decreased by rates of -8.05E-03 μ m/second and -6.66E-02 μ m/°C. Figure 3 shows the variation in the PEB's temperature profile at the wafer's center versus outer circumference. Using a monitoring wafer attached with thermocouples revealed that the wafer's edges heat up and cool down at a faster rate during the PEB process. The differing heat distribution across the wafer during the PEB thermal history plays a primary role in determining the size of the CD linewidth. Consequently, smaller CD features are found near the wafer's edges in comparison to the center.

Fig. 2. Increasing PEB (a) time and (b) temperature results in a downward trend for GL CD linewidth.

Fig. 3. (a) Temperature traces per thermocouple and (b) intrawafer temperature gradient was captured at multiple timestamps throughout the PEB process. Temperature scale is normalized per wafer at a given timestamp (t_n) .

Effects of Exposure Dose Compensation on CD Uniformity

After dialing in the optimized recipe settings for PEB temperature and time, to reduce the effect on CD linewidths from the wafer's thermal history during the PEB process, the exposure dose was customized per exposure field. By finetuning the exposure dose compensation ratio per exposure field, the impact of the post-exposure conditions on field-tofield CD uniformity can be minimized. As a proof of concept using blanket GaAs wafers, exposure dose compensation was applied to 15 fields with the largest and smallest CD linewidths to address the intra-wafer CD variation. Consequently, after dose compensation, the standard deviation of intra-wafer CD measurements on blanket GaAs wafers was reduced by 13.6% as shown in Figure 4.

The baseline data from the initial DOE was used to further dial-in the exposure dose compensation ratios for 18 exposure fields to address the PEB-induced signature shown in Figure 5. Several DOE were performed using multiple coat and develop tracks as well as lithography steppers to verify consistency of the CD measurements as well as rule out tool matching as a primary contributor to the CD variation. Moreover, the lens heating effect due to energy absorption can cause the focal plane to drift while the photoresist is being exposed [3]. This can directly affect the size of the CD linewidth and cause a high across cassette CD variation. As shown in Figure 6, the optimized exposure settings with the application of varied dose compensation ratios to 18 fields not only reduced the standard deviation of intra-wafer CD variation by 15.9% but also reduced the shift in average CD between the first and tenth wafer processed in a cassette by

92.3%. This significant reduction in wafer-to-wafer CD variation improved the stability of the photolithography process and required fewer routine dose adjustments to keep CD trends centered on the targeted value.

Fig. 4. Exposure dose compensation improved CD uniformity for blanket GaAs wafers.

Fig. 5. Optimized exposure dose compensation ratios applied to 18 exposure fields tightened intra-wafer and across cassette CD variation that resulted from the PEB-induced signature.

Fig. 6. Shift in average CD from first to tenth wafer in a cassette was significantly reduced after optimized exposure dose compensation was applied in the lithography stepper's exposure job.

Wait Time between Exposure and Post-exposure Bake

Alkaline compounds (e.g., carbon dioxide, ammonia) can diffuse onto the surface of the photoresist and subsequently neutralize the photoacids generated during the exposure process. Therefore, shortening the wait time shown in Figure 7, between the wafer's exposure on the lithography stepper and PEB-driven reaction, is important. A positive linear correlation was found between improved CD uniformity and lower wait time between the exposure and PEB processes. As shown in Figure 8, the range and standard deviation of the intra-wafer CD uniformity increased at rates of 2.19E-04 µm/minute and 6.24E-05 µm/minute respectively as wait time increased.

Based on these DOE results, in order to maintain high CD uniformity and minimal run-to-run variation, a timer was implemented within the manufacturing execution system and automated scheduler to enforce a maximum wait time between the exposure and PEB steps. The combination of the reduced wait time between exposure and PEB processes as well as optimized exposure jobs with dialed-in exposure dose compensation ratios resulted in tightening the BiHEMT devices' distributions of GL CDs measured at the postdevelop step by ~30% as shown in Figure 9. Consequently, photolithography rework rate due to out-of-control (OOC) BiHEMT GL CDs was reduced by 80%. Furthermore, wafers with inline CDs that were within the statistical process control limits continued moving downstream and had the GL pattern etched; at the optimized settings, the distribution of run-to-run CDs measured after stripping off the photoresist was tightened by ~7% as shown in Figure 10.

Fig. 7. Wait time between the exposure and PEB processes was minimized to prevent neutralization of photoacids.

Normalized Wait Time between Exposure and PEB

Fig. 8. Higher wait times between the exposure and PEB processes resulted in neutralization of photoacids which led to high GL CD linewidth variation and poor uniformity.

Fig. 9. BiHEMT GL CD distribution measured at the postdevelop step after the implementation of an automated timer and dose compensated exposure jobs in production was tightened by a factor of 1.40.

Fig. 10. At the optimal settings, the BiHEMT GL CD distribution measured at the photoresist strip step was tightened by a factor of 1.08.

CONCLUSIONS

This study provided valuable insight into the challenges of using CAMP negative tone photoresist and the necessity for optimizing the GL photolithography process to tighten CD variation. Reducing the wait time between the exposure and PEB steps improved intra-wafer, wafer-to-wafer, and lot-tolot CD variation. Intra-field CD variation was primarily influenced by the wafer's thermal history during the PEB process. The stepper's exposure recipe was optimized with exposure dose compensation to address the CD variation in fields that were most affected by the PEB-induced signature.

Addressing previously erratic CD trends and tightening die-to-die CD variation improved the process capability indices (Cpk) for the GL photolithography process and eliminated associated rework. As a result, this reduced the overall fabrication costs, chemical consumption, and sustaining resources allocated for the BiHEMT GL process. The presented experimental assessments are also applicable for identifying sources of process variation in other semiconductors' photolithography schemes to improve process capability and process control for stable CD trends and high CD uniformity. This study's results will especially be of interest for downscaling the gate length to optimize RF device performance at higher operating frequencies.

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ACRONYMS DOE: Design of Experiments GL: Gate Layer SPC: Statistical Process Control CD: Critical Dimension CAMP: Chemically Amplified PEB: Post-exposure Bake pHEMT: Pseudo-morphic High Electron Mobility Transistor HBT: Heterojunction Bipolar Transistor RF: Radio Frequency SEM: Scanning Electron Microscope PCM: Process Control Monitor UV: Ultraviolet OOC: Out-of-control