Automated Recipe Builder and Optimization of Overlay Recipes for Minimal Submicron Misalignment of Multi-layer RF Compound Semiconductor Devices

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Abstract

Overlay recipes, calibration strategies, and target designs were optimized for submicron layer-to-layer alignment with high measurement accuracy and precision for compound semiconductor devices in high-volume manufacturing. Automated recipe builder (ARB) streamlined the efficiency of auto-generating recipes for new devices and deploying optimized setups to existing recipes. Tightened statistical process control (SPC), improved process capability (Cpk), and productivity gains were achieved through recipe optimization, minimal tool measurement error, and reduction of photolithography rework from misalignment.

Key words: automation, overlay, misalignment, RF devices

Introduction

Shrinking critical dimensions for InGaP/GaAs heterojunction bipolar transistors (HBT), high electron mobility transistors (HEMT), and bipolar field effect transistors (BiFET) is crucial for enhancing design flexibility to maximize RF device performance. To address challenges of tighter overlay specifications, it is essential for accurate detection of submicron misalignment between the patterned photoresist layer and underlying layer of multi-layer devices. To address the rising challenges of tighter overlay specifications, it is essential to have advanced overlay metrology tools that can produce overlay measurements with high accuracy, precision, and throughput. Critical device parameters can be highly sensitive to overlay errors and impact the final product's electrical performance and characteristics. For instance, in RF devices, the base contact (BC) to emitter mesa (EM) defines the ledge, which is the spacing for the base emitter junction. This has a direct impact on the RF current gain of the HBT. When this spacing is less than the required specifications, RF current gain decreases and hinders device performance. As such, minimal misalignment between these two device layers is essential [1].

Various sources can affect the overall process overlay budget. Non-tool related measurement errors can be attributed to the lithography system's stage and lens, photoresist non-uniformity, track's coat and develop conditions, device topography, substrate flatness, and stress induced by upstream processes [2]. Therefore, the contribution of measurement error from the measurement tool itself must be minimized to determine appropriate overlay offset corrections to be applied within the lithography system's exposure job. For charge-sensitive devices or applications where multiple underlying layers must be simultaneously visible for measurement, optical-based tools are preferable over scanning electron microscope (SEM) tools.

In this paper, we provide an assessment of how different layers of compound semiconductor devices present its own set of challenges for obtaining accurate overlay measurements. Overlay designs and recipes on an automated optical overlay measurement system were optimized to obtain reliable registration data that minimized layer-to-layer misalignment for different compound semiconductor devices.

Overlay Recipe Optimization

Misalignment of overlay targets were evaluated using the SEM and automated optical system. Setting SEM measurements as the "golden standard," the discrepancy with overlay measurements on the optical system was reduced by optimizing its overlay recipe setup.

A. Pattern Recognition

Pattern recognition compares the pixel-level electronic registration of the stored model and live overlay target. A higher pattern recognition score cutoff requires a more accurate pattern recognition match and increases the probability of alignment to the correct global alignment and overlay target. However, lower score cutoffs were found to be more appropriate in the cases of where high grain, poor contrast, or artifacts in the wafer's background conditions caused high site-to-site or wafer-to-wafer variation.

Upon failure of pattern recognition within the field of view, automated spiral recovery widens the search rectangle and spirals to continue searching for a satisfactory pattern recognition match. Increasing the size of the pattern recognition gate for global alignment increases the risk of positioning errors and capturing background artifacts that are not reproducible from site-to-site. Hence, the pattern recognition gate was sized accordingly over a unique feature within the process control monitor (PCM) coupon with minimal site-to-site variation. For devices in which it was challenging to focus on the overlay target, off-site focus was performed. In these cases, the tool focuses on a unique feature on the same layer as the overlay target but at a recorded distance outside the overlay target's field of view before shifting back to the measurement site. Similarly, in cases where the overlay target is surrounded by identical patterns within the field of view, pattern recognition can be performed on an off-site feature with higher contrasting edges before navigating back to the measurement site.

B. Measurement Algorithms and Focus Optimization

On average, post-optimized recipes achieved higher margins which reduced the probability of selecting an incorrect edge for overlay measurement. A higher margin corresponds to reduced

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site-to-site sensitivity and improved edge detection of the overlay target across a range of gray-level contrast sensitivities. For devices with overlay features of small geometries, a two-pass slew focusing algorithm refined focus and improved detection of edge sharpness. By varying focus and examining the effects on the image signal's intensity profile, an appropriate focus algorithm was determined for the overlay recipe of each technology's layer as shown in Figure 1. However, thin film effects or optical variations may limit the accuracy of these methods for determining optimal focus based on the slope of the image's edge. The focus optimization functionality was used to auto-perform a series of test runs to determine an optimal focus offset for a given process recipe. For each recipe setup, process runs with varying focus offsets were tested for precision, tool-induced shift (TIS), total measurement uncertainty (TMU), and site time; an optimal offset was determined based upon generated statistics.

For layers with thicker photoresists, it was necessary to select a focus algorithm that accounted for a large step height between the patterned and underlying layer. For instance, the step height between the inner and outer box-in-box for via layers in Figure 2 required a dual plane measurement with two focus gates due to a photoresist thickness of several microns. Furthermore, the automated optical overlay measurement system is built to learn from past navigation and focus issues; errors encountered from initial runs of a recipe are recorded and fed forward to subsequent runs to reduce the probability of repeating the issue. For instance, the z-position of the previous run is saved as the starting z-position for future runs; this eliminates time spent on repositioning the image prior to taking future measurements and improves consistency in capturing the overlay target in focus. This adaptive navigation and focus optimization method improved the overall efficiency of running overlay measurements in high-volume manufacturing.

C. Tool-induced Shift Calibration

An asymmetric image of the measurement target would decrease the accuracy of navigating to a site location for global alignment or overlay measurement. A series of DOE measuring overlay for various layers from different technologies demonstrated that upstream processes, wafer conditions, and device topography had varying effects on site-to-site variation. TIS calibration was used to determine the site-to-site, field-to-field, and wafer-to-wafer variation that arise from asymmetries of the measurement tool components (e.g., objective aberrations, misalignment of the optical system, illumination uniformity).

Calibration strategies can be performed at the site, layer, or field level. TIS values are computed by taking the average of differences between overlay measurements performed at 0 and 180 degrees. While calibration by site improves measurement accuracy as well as detection of tool and process drifts, it results in lower throughput. Therefore, based on the severity of TIS variation per classification, the appropriate frequency of TIS calibration was selected per process recipe.

Overlay Target Design

For shrinking dimensions, photoresist fidelity tends to round off at the corners of the overlay target. It is important to maintain edge sharpness as intended by the layout design for accurate edge detection. Using a cross for the overlay target increased accuracy and precision of overlay measurements in comparison to using a box-in-box. This is because crosses maintain straight edges even when the spacing between the patterned and underlying layer becomes very narrow. By comparison, scaling down dimensions has a greater extent of photoresist rounding at the corners of inner and outer boxes. Photoresist rounding will limit the margin allotted for overlay gate placement and hence hinder measurement accuracy and precision. As shown in Figure 3, overlay registration was measured for both target designs (box-in-box and cross). Evaluation of edge profiles and sensitivity contrast was used to determine a suitable target design for each process layer.

In our case study for overlay at the contact via (CV) layer, a combination of asymmetry as well as poor contrast and focus resulted in the incorrect edge detection of the box-in-box. Moreover, minimal CV to EM misalignment is crucial for avoiding reliability issues. At CV layer, photoresist is coated over nitride that is deposited on top of the base and emitter. With the appropriate process conditions, metal 1 (M1) interconnect deposited on CV would only connect to EM. However, misalignment at the CV layer can cause the photoresist placement to shift and lead to yield loss and reliability failure. As shown in Figure 4, in the case of CV to EM misalignment, the deposited M1 layer following CV nitride etch can short the base through the epitaxy and cause M1 diffusion into the transistor. The proposed solution of using a cross structure at CV layer improved both contrast and sharpness for edge detection at the photoresist foot. As shown in Figure 5, after recipe optimization was performed for both overlay target designs (CV box-in-box and cross), the standard deviation of X and Y overlay was reduced by 58% and 20% respectively when using the cross instead of the box-in-box.

Automated Recipe Builder & Auditor

In a high-mix, high-volume manufacturing environment for device fabrication it can become challenging to manually set up and manage each overlay recipe. Each technology consists of many multi-layer devices. When an overlay recipe is optimized, it is only applied to a specific layer of that device. Propagation of recipe edits across all devices of a technology for that layer's recipe would require manually fixing each recipe by loading each device's wafer onto the stage and re-optimizing the recipe setup. However, this process can be semi-automated by using the automated recipe builder (ARB). This approach pulls the device's layout information and merges it with the optimized golden recipe setup. The golden recipe consists of global settings (e.g., grid, alignment, wafer) as well as device and layer-specific settings (e.g., site location, focus, aperture, illumination, gate). Once an inventory of robust golden recipes has been manually created, ARB can be used to effectively deploy newly optimized recipe setups for each layer of all devices within each technology.

The recipe auditor inputs a configuration file with a list of the requested parameters, cycles through all the recipes in the inventory, and generates an output file with the extracted recipe content for the requested parameters. This allowed for recipe contents to be verified after recipe edits were made or newly

optimized setups were deployed with ARB.

Conclusion

Optimization of overlay recipes on an automated optical measurement system significantly improved both accuracy and precision of submicron layer-to-layer alignment of multi-layer RF devices. Advanced techniques were implemented for building recipes with optimal focus and measurement algorithms, gate setups, tool-induced shift strategies, and designs of overlay targets to address unique process conditions at different layers within each technology's fabrication process flow. ARB and recipe auditor were implemented for off-line mass generation and deployment of optimized overlay setups as well as mass recipe verification. This eliminated the need for manual creation of overlay recipes for new devices or old recipes that require re-optimization. This significantly reduced the sustaining resources allocated toward recipe creation and editing.

Minimizing tool measurement error in the process overlay budget ensured a robust statistical process control (SPC) over inline measurements. Consequently, timely offset adjustments in the photolithography steppers' exposure jobs could be executed. As shown in Figure 6, photolithography rework due to misalignment of interconnect layers was subsequently reduced by 93% and overlay distributions were tightened by up to 25%. Furthermore, overlay distributions were tightened by 39% and 62% respectively for BC and CV layers. Minimal misalignment at these critical layers reduced reliability risks for electrical shorts. Tightened SPC, improved Cpk, and productivity gains were achieved through minimal tool measurement error, advanced recipe optimization, reduced turnaround time for inline offset adjustments, and automated mass-scale deployment of optimized setups.

References

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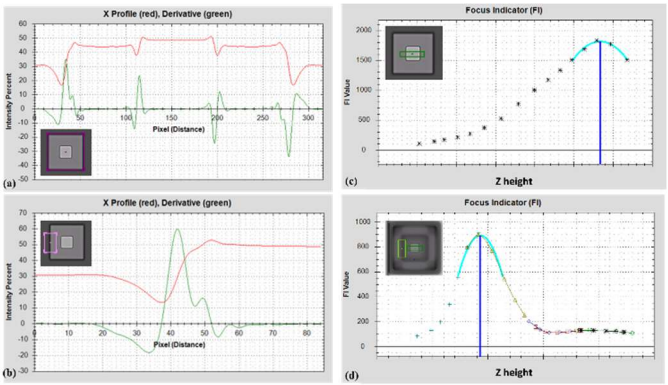

Fig. 1 Intensity profiles for measurement gates and focus indicator for single plane versus dual plane focus.

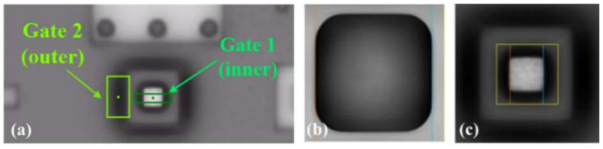

Fig. 2 (a) Dual plane measurement with a focus gate at the (b) outer box and (c) inner box.

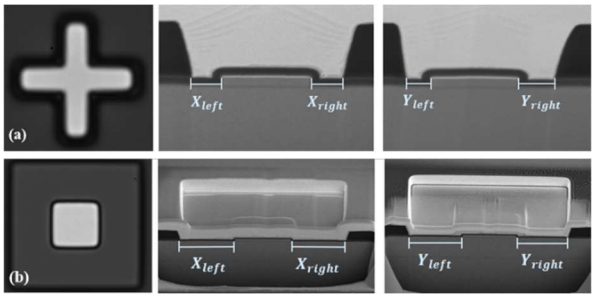

Fig. 3 Optical and SEM images of FIB cross-sections for (a) cross and (b) box-in-box as overlay target designs.

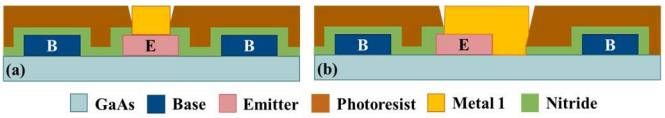

Fig. 4 Device topography after CV nitride etch and M1 interconnect deposition for (a) aligned and (b) misaligned CV layer. For the misaligned case, M1 contact with p+ GaAs shorts the base.

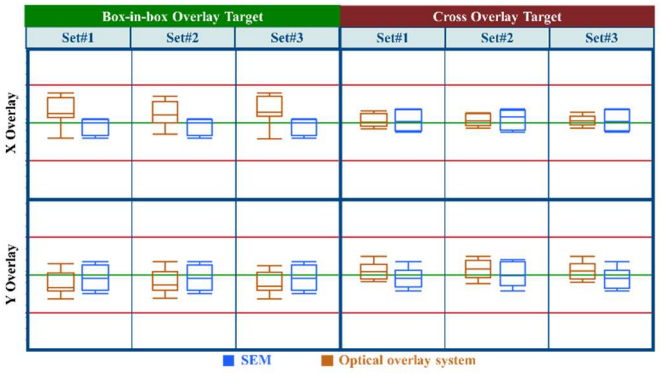

Fig. 5 SEM and optically measured X and Y overlay for target designs of a box-in-box and cross.

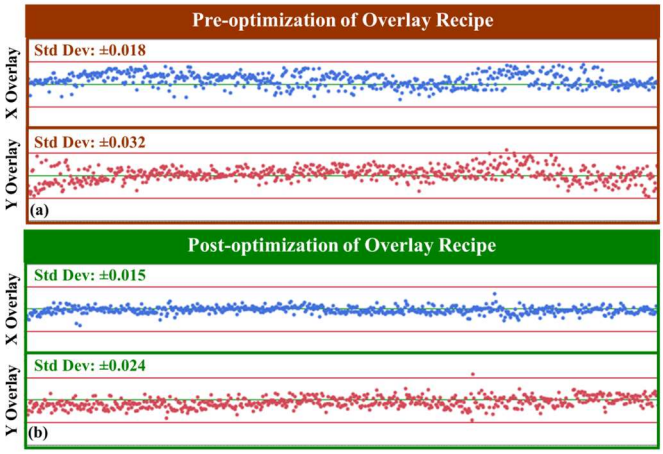

Fig. 6 X and Y overlay distributions for HBT device's M1 interconnect layer were tightened by 1.2 and 1.3 times respectively after recipe optimization.