AN892: Design Guide for Isolated DC/DC Using the Si882xx/883xx

The Si882xx/Si883xx products have integrated digital isolator channels with an isolated dc-dc controller. This application note provides guidance for selecting the external components necessary for operation of the dc-dc controller.

Digital isolation applications with primary-side supply voltage of 3.0 V ≤ V_{IN} ≤ 5.5 V and load power requirements of ≤ 2 W can use Si882xx/Si883xx products. The dc-dc controller in these products uses asymmetric half-bridge flyback circuit topology.

The figure below depicts the minimum external components required for the asymmetric half-bridge flyback converter. These are blocking capacitor C1, input capacitor C2, flyback transformer T1, diode D1, output capacitor C10, voltage sense resistors R5 and R6, and compensation network components R7 and C11.

KEY POINTS

- Digital isolation applications with primary-side supply voltage 3.0 V ≤ VIN ≤ 5.5 V and load power requirements of ≤ 2 W can use Si882xx/Si883xx products
- Guidance for selecting external components
- State equations for asymmetric half-bridge flyback topology
- Minimum external components required for asymmetric half-bridge flyback converter
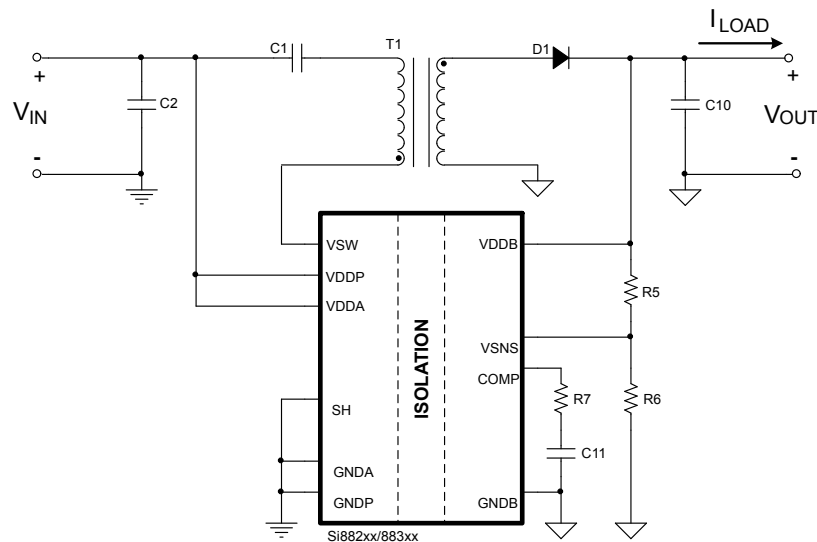
1. Simplified DC Steady State Analysis

An analysis of asymmetric half-bridge flyback converter behavior in the dc steady state yields formulas that aid the selection of values for components shown in the figure below. For this analysis, it is assumed that components are ideal, of 100% efficiency ($P_{IN}=P_{OUT}$), and that the circuit has reached equilibrium.

The figure below shows the critical components of the asymmetric half bridge flyback converter. The transformer model includes magnetizing inductance L_m and inductance leakage L_{lkg}. R_{LOAD} does not necessarily represent a physical resistor, rather it is an expression of V_{OUT}/I_{OUT}.
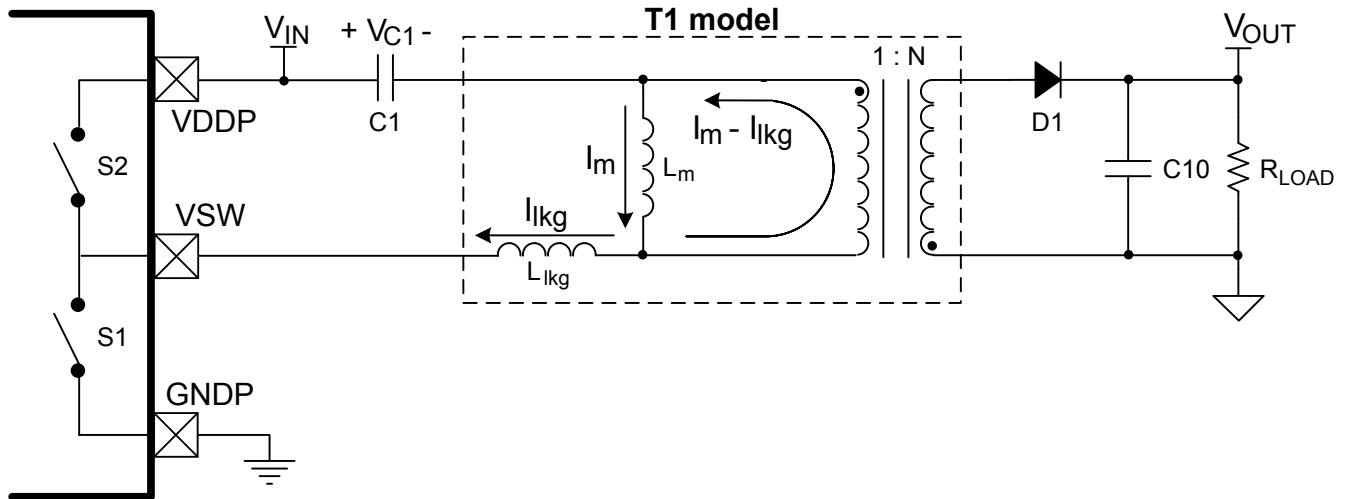

Figure 1.1. Asymmetric Half Bridge Flyback Converter

To analyze this architecture, a cycle can be divided into eight distinct operating modes. However, for dc steady state analysis, the two modes where the system operates the majority of the cycle are only required: when S1 is closed and S2 is open, and when S1 is open and S2 is closed. The figure below depicts the simplified magnetizing and leakage inductance current waveforms.
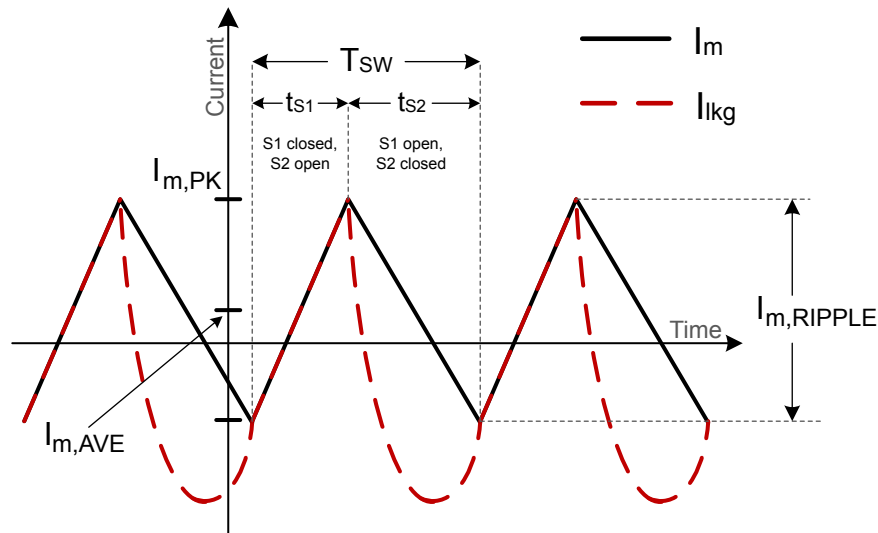

Figure 1.2. Inductor Currents

1.1 S1 Closed, S2 Open

V_{IN} is applied to the series combination of C1 and inductance L_m + L_{lkg}. As a result, current flows through inductance Lm + L_{lkg} in a linear fashion.

$$V_{IN} - V_{C1} = (L_m + L_{lkg}) \times \frac{I_{m,RIPPLE}}{t_{S1}}$$

Equation 1

Where $I_{m,RIPPLE}$ is the magnetizing current ramp during t_{S1} and t_{S1} is the time that S1 is closed.

1.2 S1 Open, S2 Closed

In this mode, a resonant tank circuit is formed by C1, L_m, and L_{lkg}. And, $-V_{C1}$ is applied across L_m + L_{lkg}. The resonant tank causes the current flowing through the leakage inductance to rise as a sinusoid while the voltage at the secondary impressed on the primary causes the current through the primary to reduce in a linear fashion. When $I_{lkg} \neq I_m$, the difference current ($I_m - I_{lkg}$) flows out of the dot on the primary side of the ideal transformer. Therefore, current must flow into the dot on the secondary side and through the diode. Governing current equations are:

$$\frac{I_{m,RIPPLE}}{t_{S2}} = \frac{-V_{OUT}}{L_m N}$$

Equation 2

$$I_{Llkg}(t) = I_m \times \sin(\omega_r t)$$

Equation 3

$$\omega_r = \frac{1}{\sqrt{L_{lkg} \times C1}}$$

Equation 4

where N and t_{S2} are the primary to secondary turns ratio and the time that S2 is closed, respectively. ω_r is the resonance tank frequency in rads/s.

The current through the diode in the secondary can be written as the difference of I_{lkg} and I_m scaled by the transformer turns ratio.

$$I_{D1} = \frac{I_{lm} - I_{lkg}}{N}$$

Equation 5

As the sinusoidal current returns to match the magnetizing current, the resonance ceases and consequently no current will flow from the dot on the primary or through the secondary into the diode.

1.3 Voltage Transfer

Let duty cycle D be defined as the ratio of time S1 is closed over the complete switching period T_{SW}:

$$D = \frac{t_{S1}}{t_{S1} + t_{S2}}$$

Equation 6

Now t_{S1} and t_{S2} can be expressed in terms of D and switching period as:

$$t_{S1} = DT_{SW}$$

Equation 7

$$t_{S2} = (1 - D)T_{SW}$$

Equation 8

and assume diode D1 has no voltage drop when conducting, the volt-second balance equation for L_{lkg} can be written as:

$$\frac{L_{lkg}}{L_{lkg} + L_m}(V_{IN} - V_{C1})DT_{SW} + (\frac{V_{OUT}}{N} - V_{C1})(1 - D)T_{SW} = 0$$

Equation 9

With the condition that $L_{lkg} \ll L_m$, Equation 9 simplifies to:

$$V_{C1} \sim = \frac{V_{OUT}}{N}$$

Equation 10

The volt-second balance equation for L_m is:

$$-\frac{V_{OUT}}{N}(1 - D)T_{SW} + \frac{L_m}{L_{lkg} + L_m}(V_{IN} - V_{C1})DT_{SW} = 0$$

Equation 11

With the condition that $L_{lkg} \ll L_m$, Equation 11 simplifies to:

$$\frac{V_{OUT} \times (1 - D)}{N} \sim = (V_{IN} - V_{C1})D$$

Equation 12

Substituting Equation 10 into Equation 12 yields the following relationships:

$$\frac{V_{OUT}}{N} \sim = V_{IN}D$$

Equation 13

$$V_{C1} \sim = V_{IN}D$$

Equation 14

1.4 Magnetizing Current

During the t_{S1} portion of the cycle (S1 closed, S2 open), V_{IN} charges C1 in a linear fashion. Rearranging Equation 1 and substituting Equation 7 and Equation 14, ripple magnetizing current is:

$$I_{m,RIPPLE} = \frac{(V_{IN} - V_{C1})t_{S1}}{L_m + L_{lkg}} = \frac{(V_{IN} - V_{IN}D)t_{S1}}{L_m + L_{lkg}} = \frac{V_{IN}D(1-D)T_{SW}}{L_m + L_{lkg}}$$

Equation 15

The average magnetizing current is related to the output current as:

$$I_{m,AVE} = I_{LOAD}N$$

Equation 16

The peak magnetizing current is given by:

$$I_{m,PK} = I_{m,AVE} + \frac{V_{IN}D(1-D)T_{SW}}{2(L_m + L_{lkg})}$$

Equation 17

Si882xx/Si883xx controller limits the peak magnetizing current to approximately 3 A. If more current than 3 A is sensed during S1 on and S2 off mode, the controller immediately switches to the S1 off and S2 on mode. The controller maintains the same switching period, but reduces the duty cycle D to limit peak current.

1.5 Input Capacitor

The purpose of C2 input capacitor is to provide current during switching cycles. During S1 closed, S2 open, C2 provides current to C1 in series with $L_m + L_{lkg}$.

$$I_{IN} = I_{m,AVE}D = I_{LOAD}DN$$

Equation 18

During the t_{S2} portion of the cycle (S1 open, S2 closed), V_{IN} recharges C2. The voltage ripple on C2 can be written as:

$$V_{IN,RIPPLE} = \frac{I_{C2}(1-D)T_{SW}}{C2}$$

Equation 19

Substituting Equation 18 into 19:

$$V_{IN,RIPPLE} = \frac{I_{LOAD}D(1-D)T_{SW}N}{C2}$$

Equation 20

1.6 Diode and Output Capacitor

Current flows through D1 only during the $(1–D)T_{SW}$ portion of the steady state cycle. During the DT_{SW} portion of the cycle, I_{LOAD} is sourced solely by the output capacitor C10. Output voltage ripple on C10 can be calculated by:

$$V_{OUT,RIPLLE} = \frac{I_{LOAD}DT_{SW}}{C10}$$

Equation 21

The average current on D1 is equal to the load current:

$$I_{D1,AVE} = I_{LOAD}$$

Equation 22

When D1 is reverse biased, it must withstand:

$$V_{D1,REV} = V_{IN}(1 - D)N + V_{OUT}$$

Equation 23

When operating the converter at high ambient temperatures (>70 °C), low-leakage rectifying diodes are needed in the power supply output. The following table describes a diode that was tested in the circuit and will fulfill these requirements:

Table 1.1. DC-DC Supply Output Rectifier Diode for High Working Temperatures

Mfr P/N	Mfr / Website	Vf(max)	Leakage Current (Reverse Current, Max)
PMEG6020ELR	Nexperia www.nexperia.com	760 mV @ 2 A, 25 °C	120 μA typ @ VR = 60 V, Ti = +125 °C, Short duration pulse test used to minimize self-heating effect.

The other low-leakage rectifying diode tested was the MBR0580S1. Since the MBR0580S1 has only a 0.5 A current rating, the MBR0580S1 can only be used when the application allows.

1.7 VSNS Voltage Divider

For the purpose of selecting sense resistors (R5/R6), the entire dc-dc converter can be modeled as a non-inverting amplifier as shown in the figure below. Notice that the non-inverting input, supply voltage (V+), and output voltage of the amplifier correspond to the internal 1.05 V reference, V_{IN} and V_{OUT}, of the dc-dc converter.
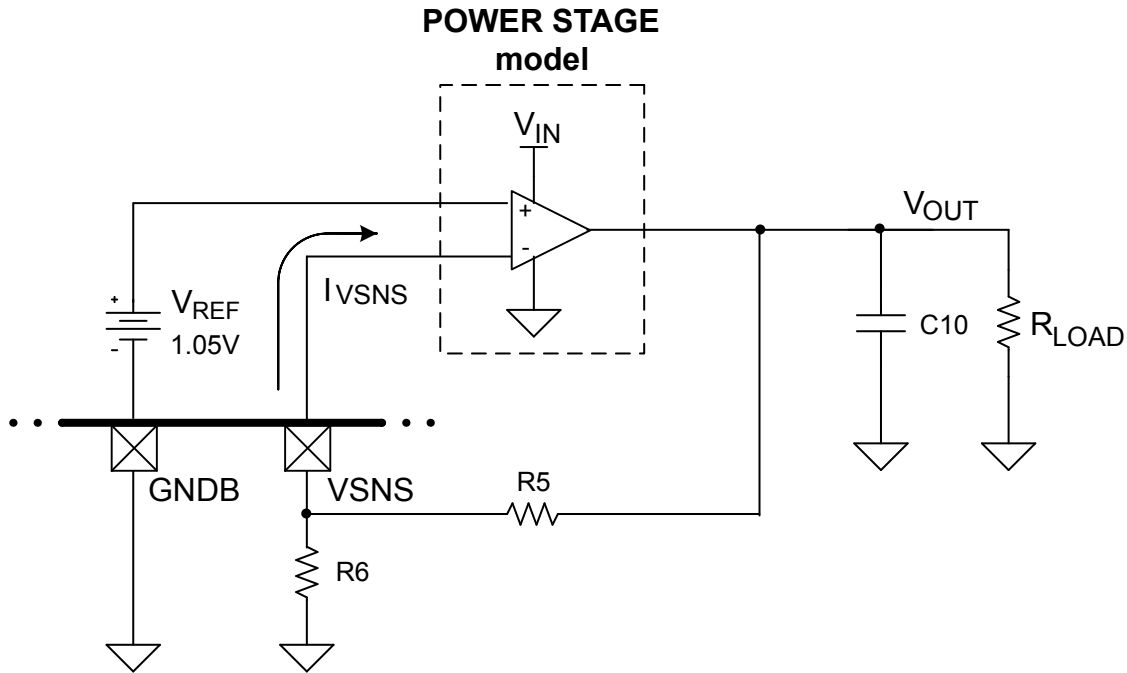

Figure 1.3. Simplified V$_{OUT}$ Gain Model

Assuming infinite dc gain and applying KCL at the inverting input of the amplifier, V_{OUT} can be expressed as:

$$V_{OUT} = 1.05(\frac{R5}{R6} + 1) + R5 \times I_{VSNS}$$

Equation 24

where I_{VSNS} represents the input offset current at VSNS pin. From Equation 24, it can be observed that a very large R5 could reduce the output voltage accuracy.

2. Dynamic Response

The Si882xx/3xx start-up response consists of three regions of operation: Soft-Start (SS), Proportional Mode (P-Mode), and Proportional Integral Mode (PI-mode). The figure shows a typical V_{OUT} response during startup.
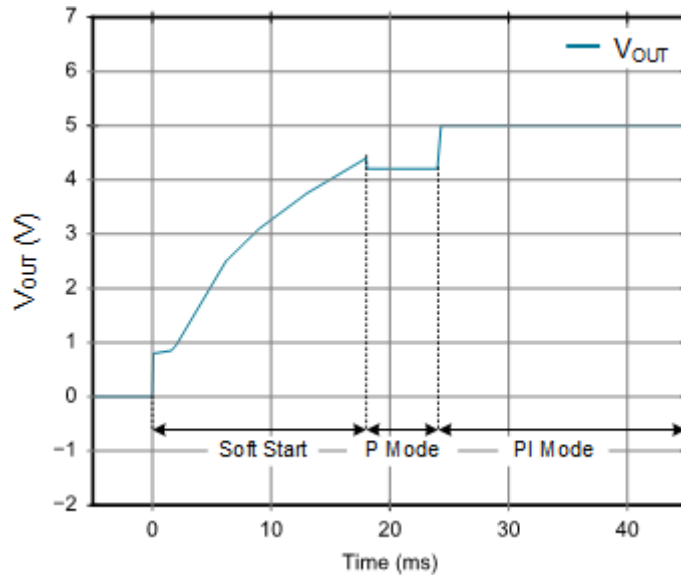
Figure 2.1. V_{OUT} during Start Up

2.1 Soft Start

In soft start mode, the dc-dc peak current limit is gradually increased to limit the sudden demand of current needed from the primary supply. This mode of operation guarantees that V_{OUT} monotonically increases and minimizes the probability of a voltage overshoot. Once 90% of the final V_{OUT} is reached, soft-start mode ends and Proportional (P) Mode starts. The total duration of soft start is load-dependent as it affects how many switching cycles are required for V_{OUT} to reach 90% of final value. In this mode of operation, the voltage feedback loop is inactive and, hence, loop stability is not a concern.

2.2 Proportional Mode

Once the secondary side senses 90% of V_{OUT}, the control loop begins its P-mode operation. During this mode of operation the dc-dc converter closes the loop (dc-dc converter secondary side communicates with the primary side) and therefore, analyzing the loop stability is required.

The figure below shows a simplified block diagram of voltage sensed feedback control. The gm_p represents the equivalent modulator and power stage transconductance of the dc-dc converter and resistors R5 and R6 are the feedback resistors used to sense V_{OUT}. C10 is the output capacitor, and R_{LOAD} represents output load. Parameter gm_{fb} and $R_{o,gmfb}$ are the effective error amplifier transconductance and the error amplifier output resistance, respectively. During the P-Mode, an integrated resistor R_{INT} is connected to the COMP pin. R7 and C11 are external components connected to the COMP pin used in P-I mode.
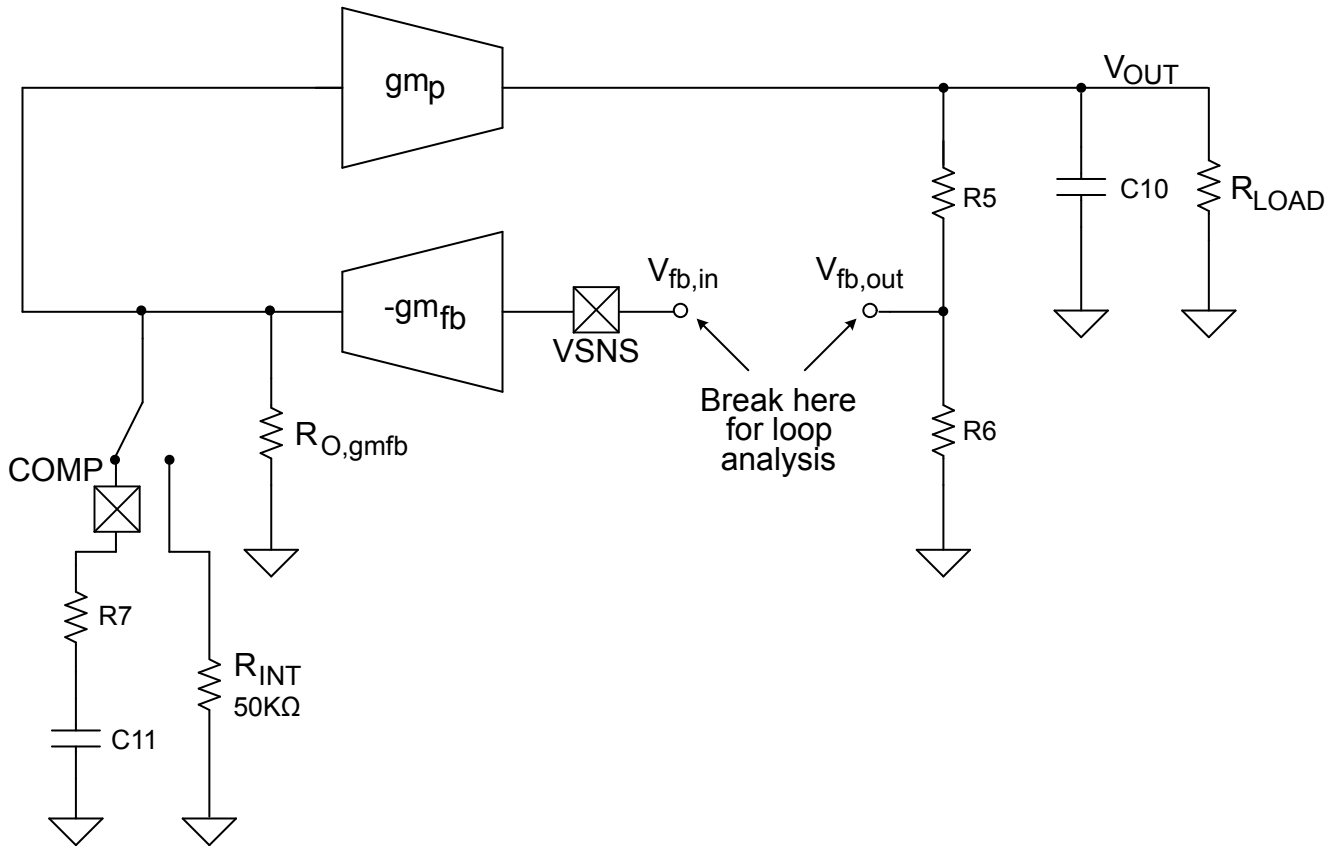
Figure 2.2. Simplified Voltage Sense Feedback Loop

For stability analysis, the loop at the input of the error amplifier is broken to obtain the small-signal transfer function from $V_{fb,in}$ to $V_{fb,out}$:

$$H_p(s) = \frac{V_{fb,out}}{V_{fb,in}} = A_{DC,P}\frac{1}{(1+\frac{s}{p})}$$

Equation 25

$$pd^\sim = \frac{1}{R_{LOAD}C_{10}}$$

Equation 26

$$A_{DC,P} = -\frac{R6}{R5+R6}gm_{fb}(R_{INT}||R_{o,gmfb}) \times gm_p(R_{LOAD}||(R5+R6))$$

Equation 27

$$gm_{fb} = \frac{gm_{ea}}{gm_{ea}(R5||R6) + 1}$$

Equation 28

gm_{ea} is the error amplifier transconductance. For the Si882xx/Si883xx, $gm_{ea} \sim= 1\times10^{-3}$, $R_{INT} \sim= 50$ kΩ, and $R_{o,gmfb} >> R_{INT}$. If R5 and R6 are chosen such that their parallel resistance is sufficiently larger than $1/gm_{ea}$, Equation 28 simplifies to:

$$gm_{fb}\sim = \frac{1}{(R5||R6)}$$

Equation 29

Typically, $R_{LOAD} << (R5 + R6)$ and gm_p is approximately 3/N. The dc gain in P-mode simplifies to:

$$A_{DC,P}\sim = -\frac{50 \times 10^3 \times 3R_{LOAD}}{R5 \times N}$$

Equation 30

Notice that the dc gain of P mode is proportional to R_{LOAD} and inversely proportional to R5. At heavy loads (small R_{LOAD}), a very large R5 could significantly increase the output voltage error as the dc gain reduces. Conversely, a very small R5 increases power consumption and gm_{fb} variability due to higher dependency on gm_{ea}, which can significantly vary more than 1/(R5||R6) over temperature or from part to part. The total duration of this mode is approximately 7 ms.

2.3 Proportional Integral Mode

After P-mode, the controller switches to PI-mode, the steady state and final operation mode. During this mode of operation, the error amplifier drives an impedance that consists of the series combination of resistor R7 and capacitor C11. To achieve a smooth transition between P and PI modes, it is recommended to set R7 to match R_{INT}. R7 and C11 are connected to the COMP pin.

$$R7 = R_{INT\sim} = 50x10^3$$

Equation 31

In PI-mode, the loop transfer is given by:

$$H_{PI}(s) = A_{DC,PI} \frac{(1 + \frac{s}{Z1})}{(1 + \frac{s}{p1}) \times (1 + \frac{s}{p2})}$$

Equation 32

where

$$p1\sim = \frac{1}{R_{o,gmfb}C11}$$

Equation 33

$$Z1\sim = \frac{1}{R7C11}$$

Equation 34

$$p2\sim = \frac{1}{R_{LOAD}C10}$$

Equation 35

$$A_{DC,PI} = -\frac{R_{o,gmfb}gm_p R_{LOAD}}{R5}$$

Equation 36

Notice that the loop transfer function in PI-Mode has an additional pole-zero pair when compared with P-Mode. In addition, the loop DC-gain is much higher in PI-Mode than in P-Mode due to $R_{o,gmfb} \gg R_{INT}$.

The figure below shows the magnitude Bode plot of the loop in PI mode.
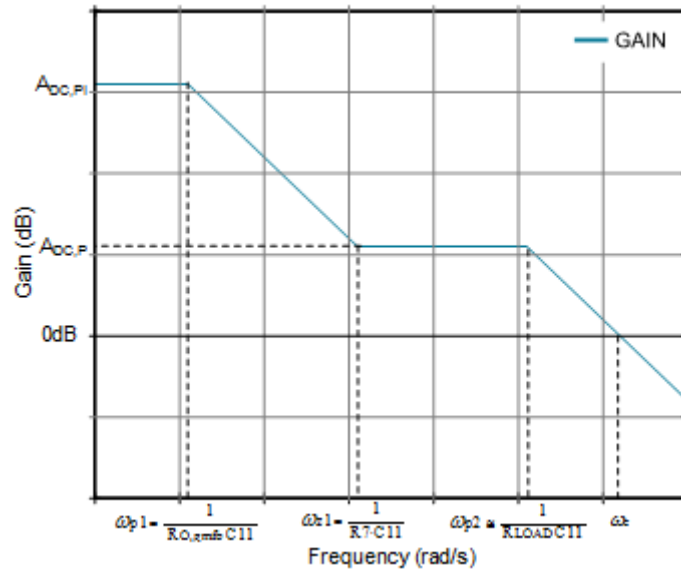
Figure 2.3. Simplified Transfer Function PI Mode

3. Design Example

Design Example

Consider the desired requirements listed in the table below.

Table 3.1. Design Requirements

Parameter	Value
Input Voltage	5.0 V ± 10%
Output Voltage	5.0 V
Input Voltage Ripple	≤ 150 mV
Output Voltage Ripple	≤ 50 mV
Maximum Output Current	400 mA
Switching Frequency	250 kHz

3.1 Transformer Design

The design of a transformer for the asymmetric half-bridge flyback converter is very similar to the design of a flyback transformer operating in continuous current mode. This section provides a starting point for the transformer design which is often an iterative process.

Equation 13 establishes the relationship between turns ratio N and duty cycle D. For this design, D=0.25 was chosen. The formulas derived in the dc steady state section are based on ideal elements. In practice, a larger duty cycle is expected due to losses in the parasitics. Accounting for forward voltage drop across D1 of 0.5 V and solving Equation 13 for turns ratio:

$$N\sim = \frac{V_{OUT} + V_{fD1}}{V_{IN}D} = \frac{5 + 0.5}{5 \times 0.25} \sim = 4.4$$

Equation 37

A 1:4 turns ratio was chosen.

The next parameter to choose is the primary inductance. Equation 16 gives the average magnetizing current.

$$Im_{AVE} = NI_{LOAD} = 4(0.4) = 1.6A$$

Equation 38

The equation below shows that magnetizing current ripple is inversely proportional to primary inductance. There are considerations for choosing the magnitude of the magnetizing current ripple. Choosing a very small primary inductance leads to a large current ripple. Care must be taken not to approach the cycle-by-cycle current limit of approximately 3 A. For this design, peak current was chosen not to exceed 2.5 A at specified maximum I_{LOAD}. A ripple current of 1.8 A was targeted. Rearranging Equation 15,

$$L_m + L_{lkg} = \frac{V_{IN}D(1 - D)T_{SW}}{I_{m, RIPPLE}} = \frac{5 \times 0.25(0.75)4x10^{-6}}{1.8} = 2.08 \mu H$$

Equation 39

The result of the equation above suggests that the combination of magnetizing current and leakage inductance should be 2.08 µH. Leakage inductance is unavoidable in transformer design, and it should be minimized for the best energy transfer in an asymmetric half bridge flyback converter. A transformer was designed with a primary inductance of 2 µH and a leakage inductance of ≤100 nH. The figure below shows the expected magnetizing current during the portion of the cycle in which S1 is closed and S2 is open.
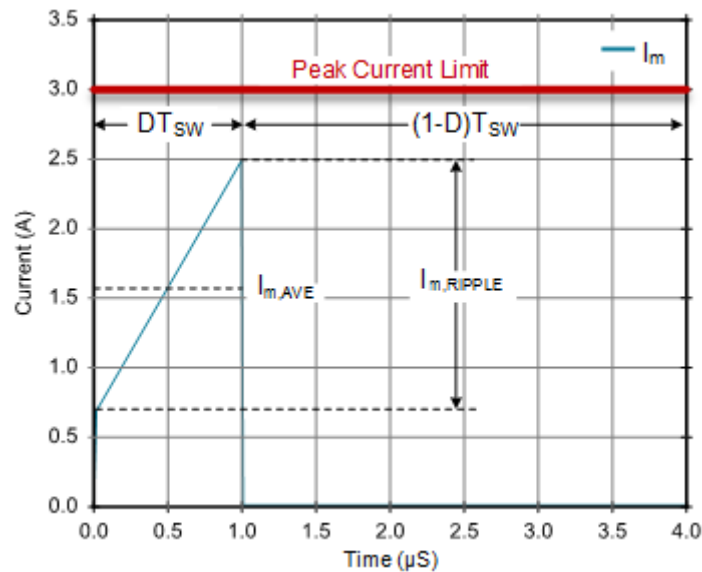

Figure 3.1. Magnetizing Current

3.2 C1 Selection

When S2 is closed, a resonant current in the primary is developed with frequency given by Equation 4. To ensure zero current switching of the diode by the time S1 closed, S2 open mode begins, C1 should be chosen so that at least half of the resonant period is completed in $(1–D)T_{SW}$ time.

$$f_r \geq \overline{(1 - D)T_{SW}}$$

Equation 40

Combining Equation 4 and Equation 40 and solving for C1:

$$C1 \leq \frac{1}{L_{lkg}}(\frac{(1 - D)T_{SW}}{\pi})^2 \approx 9.1\,uF$$

Equation 41

The next standard size capacitor 10 μF was chosen.

3.3 D1 Selection

Equations 22 and 23 define the requirements for selecting D1. Substituting into Equation 22,

$$I_{D1,AVE} = I_{LOAD} = 0.4A$$

Equation 42

Diode current capacities are usually specified in rms. Assuming a half wave sinusoid current through D1, consider the translation of average to rms:

$$I_{D1,RMS} = I_{D1,AVE}(\frac{\pi}{2\sqrt{2}}) = 0.444A$$

Equation 43

Substituting into Equation 23, consider using the maximum expected V_{IN} as the worst case requirement for reverse biasing:

$$V_{D1,REV} = V_{IN,MAX} \times (1 - D) \times N + V_{OUT} = 5.50(0.75)4 + 5 = 21.5\,v$$

Equation 44

Equations 23 and 44 do not include the voltage spike due to the interaction of the diode capacitance and leakage inductance. As a result, a diode with a larger withstanding voltage is required in practice. When selecting D1, Schottky diodes are the preferred choice due to their low forward voltage as it minimizes the associated power loss.

A 1 A, 40 V Schottky diode was selected. Please note that the low-leakage diode is required for high working temperature application. Please refer to 1.6 Diode and Output Capacitor and Table 1.1 DC-DC Supply Output Rectifier Diode for High Working Temperatures on page 6 for details.

3.4 C10 Selection

C10 is inversely proportional to output voltage ripple and sets the crossover frequency of control loop gain. It is suggested to use the minimum size capacitor to meet output voltage ripple requirements. Rearranging Equation 21,

$$C10 = \frac{I_{LOAD}DT_{SW}}{V_{OUT,RIPPLE}} \approx \frac{0.4 \times 0.25 \times 4x10^{-6}}{0.05} \approx 8\mu F$$

Equation 45

A 10 μF capacitor was chosen.

3.5 C2 Selection

In most applications, V$_{IN}$ also supplies the VDDA pin that powers the dc-dc controller and primary-side digital isolator circuitry. It is recommended to minimize voltage ripple at VDDA. Solving Equation 20:

$$C2 \geq \frac{I_{LOAD}D(1-D)T_{SW}N}{V_{IN, RIPPLE}} \geq \frac{0.4 \times 0.25 \times 0.75 \times 4x10^{-6} \times 4}{0.15} \geq 8\mu F$$

Equation 46

A 10µF capacitor was chosen.

3.6 R5 and R6

The ratio of R5 and R6 is determined by the 5 V output voltage requirement. To reduce the dependence of feedback gain on the internal error amplifier transconductance, it is recommended to have the parallel combination resistance to be ≥ 10 kΩ. Higher values of R5 + R6 reduce power loss through the divider, but at the expense of increasing output voltage error due to I$_{VSNS}$ which varies part to part. So R5 and R6 are chosen to target 10 kΩ parallel resistance.

$$10x10^3 = \frac{R5 \times R6}{R5 + R6}$$

Equation 47

$$5 = 1.05(\frac{R5}{R6} + 1)$$

Equation 48

Substituting Equation 47 into Equation 48 and solving for R6,

$$10x10^3 = \frac{3.76R6}{4.76}, R6 = 12.66x10^3, R5 = 48.1x10^3$$

Equation 49

The nearest 1% resistor to 12.66 kΩ is 12.7 kΩ. However, setting R5 to either 47.5 kΩ or 48.7 kΩ does not target exactly 5 V as well as other 1% resistor pairs. A better match was found with R6=13.3 kΩ and R5=49.9 kΩ.

3.7 Compensation Network

The compensation network is comprised of R7 and C11. R7 is fixed to match R$_{INT}$ and 49.9 kΩ is the nearest 1% resistor value. The C11 places the compensation zero in relationship to the crossover frequency. The equation for crossover frequency can be obtained by multiplying the P-mode gain (Equation 30) by the frequency of the pole created by R$_{LOAD}$ and C10 (Equation 35):

$$f_{c\~} = \frac{50x10^3 \times 3R_{LOAD}}{R5 \times N} \times \frac{1}{2 \times R_{LOAD} \times C10} = 12.1 kHz$$

Equation 50

To achieve good phase margin, it is suggested to place the zero between 1/4th to 1/10th of the estimated crossover frequency. The zero placement was chosen to lead the crossover frequency by a factor of 6.

$$C11 = \frac{6}{2f_c \times R7} = \frac{6}{2 \times 12.1x10^3 \times 49.9x10^3} = 1.58nF$$

Equation 51

A 1.5 nF capacitor was chosen.

3.8 Design Summary

Table 3.2 Design Summary on page 17 shows the component selection that meet the design requirements.

Table 3.2. Design Summary

Part Reference	Description	Manufacturer	Manufacturer Part Number
C1 C2 C10	CAP, 10 µF, 10 V, ±10%, X7R, 1206	Venkel	C1206X7R100-106K
C11	CAP, 1.5 nF, 16 V, ±10%, X7R, 0603	Venkel	C0603X7R160-152K
D1	DIO, FAST, 40 V, 1.0 A, SOD-128	Panasonic	DB2440100L
R5 R7	RES, 49.9K, 1/10W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-4992F
R6	RES, 13.3K, 1/16W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-1332F
T1	TRANSFORMER, POWER, FLYBACK, 2.0 µH PRIMARY, 100 nH LEAKAGE, 1:4, 1 TAP, SMT	UMEC	UTB02185S

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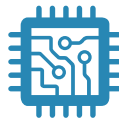
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