PRELIMINARY PRODUCT SUMMARY

Si469xx/xxC: High-Performance Automotive Digital Radio Coprocessor for HD Radio™, DAB/DAB+, DRM, and CDR

The Si469xx/xxC is a high-performance, multi-standard, multi-channel digital radio coprocessor. Supporting up to four channels, the Si469xx/xxC enables reception, decode, and playback of digital radio broadcasts by demodulating RF signals, decoding encoded audio, and seamlessly linking multiple audio streams to minimize the effects of switching between digital and analog AM/FM streams from multiple antennas. The Si469xx/xxC supports Maximal Ratio Combining (MRC), radio services, and background scan. When combined with Skyworks' Si479xx Hybrid SDR tuners, system designers benefit from unparalleled scalability and configurability allowing a single PCB design to support all global regions and a full range of performance segments. A customer-programmable MCU, Digital Data Stream Interface (DDSI), Demod/Tuner Manager, two SPI/I^2C interfaces for Host Control, and automatic power-on-reset and self-boot simplify hardware and software design and reduce system cost.

Applications

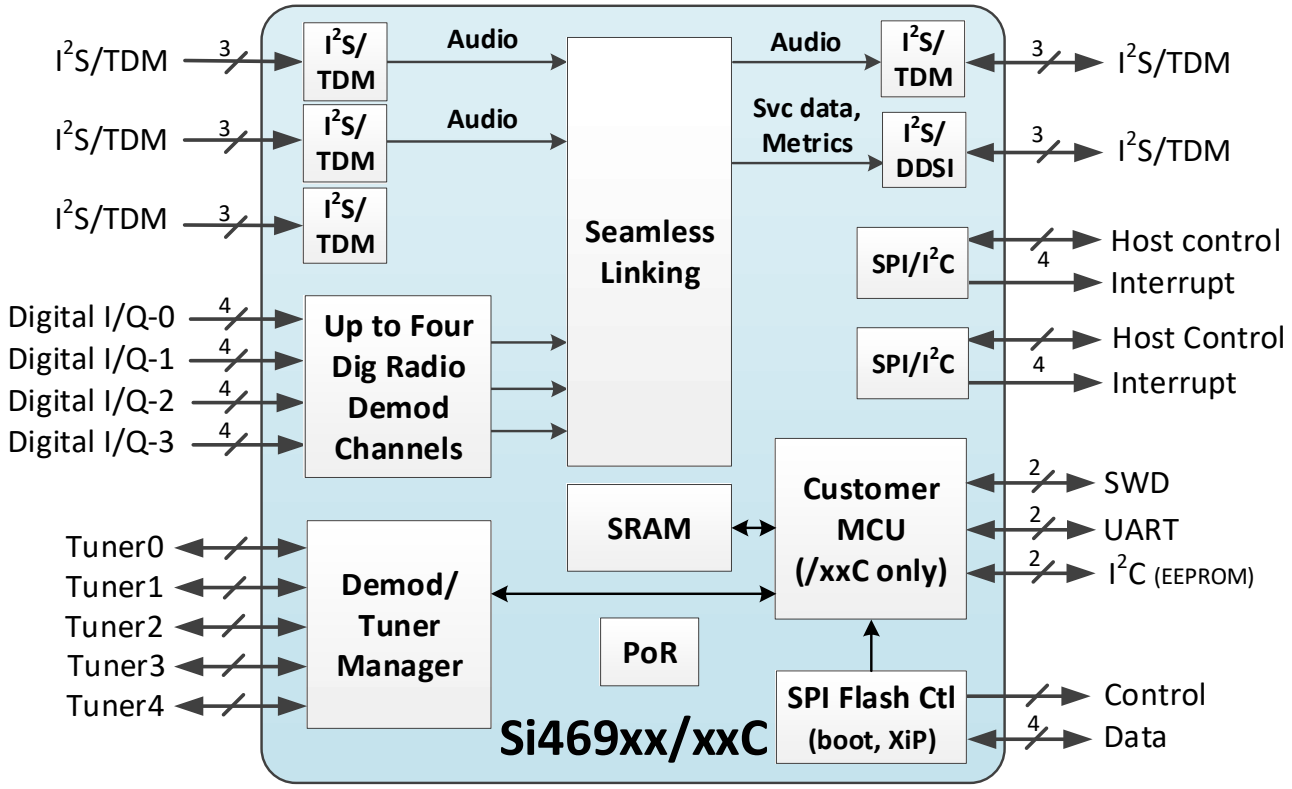
- OEM automotive infotainment systems
- Remote Tuner Modules/Smart Antennas
- Aftermarket car radio systems

Features

- Multi-standard, multi-channel digital radio coprocessor
  - 2-, 3-, and 4-channel variants
  - Digital radio demodulation
  - Audio decoding
  - Seamless linking
  - Tuner/Channel management
- 2-, 3-, and 4-channel HD Radio™ coprocessor
  - Si469x1/x1C only
  - High-Definition Coding (HDC) audio source decoder
  - FM HD1, HD2, HD3 multicast support
  - Station Information Service (SIS) Support
  - Program Service Data (PSD)
  - Advanced Application Services (AAS) Payload for data applications
- 2-, 3-, and 4-channel DAB/DAB+ Coprocessor
  - Si469x2/x2C only
  - Integrated DAB/DAB/FM time and level alignment and seamless blending
  - FIC decoder
  - Full support for data services
- 2-, 3-, and 4-channel DRM coprocessor
  - Si469x4/x4C only
  - Supports DRM in AM and FM bands
  - FAC and SDC decoder
  - Full support for data services
- 2-, 3-, and 4-channel CDR Coprocessor
  - Si469x3/x3C only
  - Audio decoder with Dynamic Resolution Adaptation (DRA), DRA+
  - Data Services
- Integrated Demod/Tuner Manager controls tuner and channel processing
- Audio Interface
  - Digital Data Stream Interface (DDSI) optimally packetizes high-payload, non-audio data (e.g., LOT/MOT) to interface to A2B™ or to a DSP over I^2S.
  - Three I^2S/TDM Audio inputs
  - Two I^2S/TDM Audio outputs
- Integrated, customer-programmable ARM Cortex M3 MCU ("C" parts only)
- Maximal Ratio Combining (MRC) for antenna diversity, available via software package for each standard
- No external RAM needed
- Serial Flash Memory interface for application program load with support for Quad SPI flash and OTA updates
- Autonomous self-boot from Flash for accelerated time to audio
- Support for Si479xx Zero-IF digital up to 744.1875K samples per second
- Two SPI/I^2C interfaces for Host Control
- UART interface allows control of XM/SDARS
- Reference clock input
- 88-pin, 12 x 12 x 0.85 mm QFN with 0.5 mm pad pitch
- AEC-Q100 qualified

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Functional Block Diagram



2. Pin Descriptions

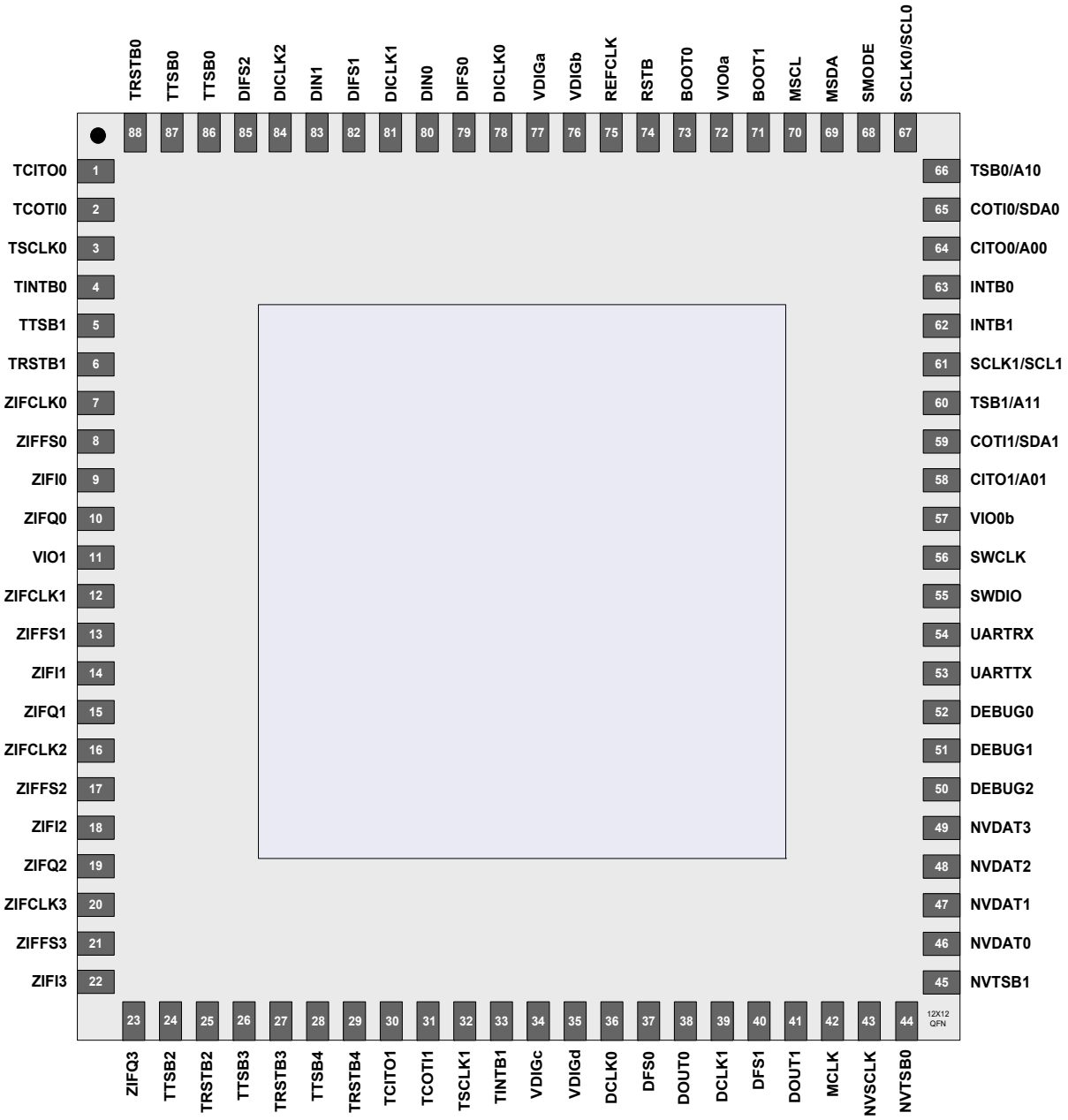


Figure 1. Si469xx/xxC Pins

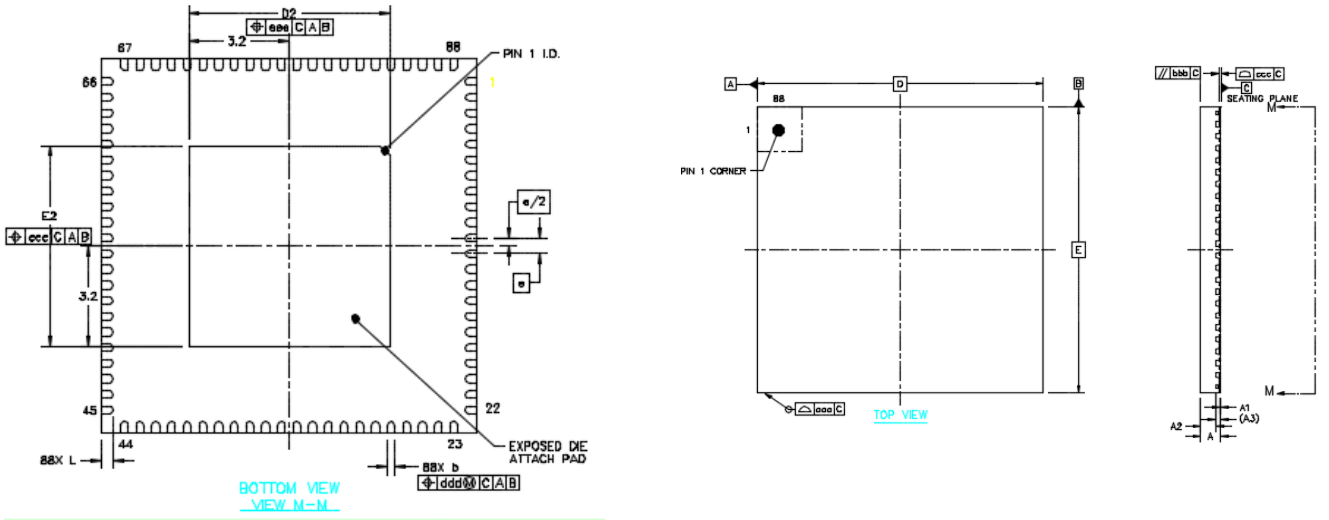
Table 1. Si469xx/xxC Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
1	TCITO0	I	VIO1	Tuner SPI 0 data, controller-in / target-out
2	TCOTI0	O	VIO1	Tuner SPI 0 data, controller-out/target-in
3	TSCLK0	O	VIO1	Tuner SPI 0 clock
4	TINTB0	I	VIO1	Tuner SPI 0 Interrupt, active low
5	TTSB1	O	VIO1	Tuner 1 SPI target select, active low
6	TRSTB1	O	VIO1	Tuner 1 reset, active low
7	ZIFCLK0	I	VIO1	ZIF clock input for coprocessor Channel 0
8	ZIFFS0	I	VIO1	ZIF frame input for coprocessor Channel 0
9	ZIFI0	I	VIO1	ZIF I-data input for coprocessor Channel 0
10	ZIFQ0	I	VIO1	ZIF Q-data input for coprocessor Channel 0
11	VIO1	Supply	VIO1	I/O supply for Tuner Interfaces
12	ZIFCLK1	I	VIO1	ZIF clock input for coprocessor Channel 1
13	ZIFFS1	I	VIO1	ZIF frame input for coprocessor Channel 1
14	ZIFI1	I	VIO1	ZIF I-data input for coprocessor Channel 1
15	ZIFQ1	I	VIO1	ZIF Q-data input for coprocessor Channel 1
16	ZIFCLK2	I	VIO1	ZIF clock input for coprocessor Channel 2
17	ZIFFS2	I	VIO1	ZIF frame input for coprocessor Channel 2
18	ZIFI2	I	VIO1	ZIF I-data input for coprocessor Channel 2
19	ZIFQ2	I	VIO1	ZIF Q-data input for coprocessor Channel 2
20	ZIFCLK3	I	VIO1	ZIF clock input for coprocessor Channel 3
21	ZIFFS3	I	VIO1	ZIF frame input for coprocessor Channel 3
22	ZIFI3	I	VIO1	ZIF I-data input for coprocessor Channel 3
23	ZIFQ3	I	VIO1	ZIF Q-data input for coprocessor Channel 3
24	TTSB2	O	VIO1	Tuner 2 SPI target select, active low
25	TRSTB2	O	VIO1	Tuner 2 reset, active low
26	TTSB3	O	VIO1	Tuner 3 SPI target select, active low
27	TRSTB3	O	VIO1	Tuner 3 reset, active low
28	TTSB4	O	VIO1	Tuner 4 SPI target select, active low
29	TRSTB4	O	VIO1	Tuner 4 reset, active low
30	TCITO1	I	VIO1	Tuner SPI 1 data, controller-in/target-out
31	TCOTI1	O	VIO1	Tuner SPI 1 data, controller-out/target-in
32	TSCLK1	O	VIO1	Tuner SPI 1 clock
33	TINTB1	I	VIO1	Tuner SPI 1 interrupt, active low
34	VDIGc	Supply	VDIG	Core/digital supply
35	VDIGd	Supply	VDIG	Core/digital supply
36	DCLK0	IO	VIO0	Host I^2S 0 clock
37	DFS0	IO	VIO0	Host I^2S 0 frame sync
38	DOUT0	O	VIO0	Host I^2S 0 data output
39	DCLK1	IO	VIO0	Host I^2S 1 clock
40	DFS1	IO	VIO0	Host I^2S 1 frame sync
41	DOUT1	O	VIO0	Host I^2S 1 data output
42	MCLK	O	VIO0	System clock for external I^2S DAC
43	NVSCLK	O	VIO0	Serial flash SPI clock
44	NVTSB0	O	VIO0	Serial flash SPI target select 0, active low
45	NVTSB1	O	VIO0	Serial flash SPI target select 1, active low

Table 1. Si469xx/xxC Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
46	NVDAT0	IO	VIO0	Serial flash SPI data 0
47	NVDAT1	IO	VIO0	Serial flash SPI data 1
48	NVDAT2	IO	VIO0	Serial flash SPI data 2
49	NVDAT3	IO	VIO0	Serial flash SPI data 3
50	DEBUG2	IO	VIO0	Debug port 2
51	DEBUG1	IO	VIO0	Debug port 1
52	DEBUG0	IO	VIO0	Debug port 0
53	UARTTX	O	VIO0	UART transmit
54	UARTRX	I	VIO0	UART receive
55	SWDIO	I/IO	VIO0	Serial wire debug I/O
56	SWCLK	I	VIO0	Serial wire debug clock
57	VIO0b	Supply	VIO0	I/O supply for host interfaces
58	CITO1/A01	O/I	VIO0	Secondary host control SPI (1) data, controller-in / target-out / I^2C 1 A0 address select
59	COTI1/SDA1	I/IO	VIO0	Secondary host control SPI (1) data, controller-Out / target-in / I^2C 1 data input/output
60	TSB1/A11	I	VIO0	Secondary host control SPI (1) target select / I^2C 1 A1 address select
61	SCLK1/SCL1	I	VIO0	Secondary host control SPI (1) clock input / I^2C 1 clock input
62	INTB1	O	VIO0	Host interrupt 1, active low
63	INTB0	O	VIO0	Host interrupt 0, active low
64	CITO0/A00	O/I	VIO0	Primary host control SPI (0) control in target out / I^2C 0 A0 address select
65	COTI0/SDA0	I/IO	VIO0	Primary host control SPI (0) data, controller-out / target-in / I^2C 0 data input/output
66	TSB0/A10	I	VIO0	Primary host control SPI (0) target select (active low) / I^2C 0 A1 address select
67	SCLK0/SCL0	I	VIO0	Primary host control SPI (0) clock input / I^2C 0 clock input
68	SMODE	I	VIO0	Set mode of primary host control serial port (0 = SPI, 1 = I^2C)
69	MSDA	IO	VIO0	Memory data for I^2C EEPROM
70	MSCL	O	VIO0	Memory clock for I^2C EEPROM
71	BOOT1	I	VIO0	Boot control 1
72	BOOT0	I	VIO0	Boot control 0
73	VIO0a	Supply	VIO0	I/O supply for host interfaces
74	RSTB	I	VIO0	Host controlled reset, active low
75	REFCLK	I	VIO0	Reference clock
76	VDIGb	Supply	VDIG	Core / digital supply
77	VDIGa	Supply	VDIG	Core / digital supply
78	DICLK0	I	VIO1	Tuner audio I^2S 0 clock
79	DIFS0	I	VIO1	Tuner audio I^2S 0 frame sync
80	DIN0	I	VIO1	Tuner audio I^2S 0 data input
81	DICLK1	I	VIO1	Tuner audio I^2S 1 clock
82	DIFS1	I	VIO1	Tuner audio I^2S 1 frame sync
83	DIN1	I	VIO1	Tuner audio I^2S, 1 data input
84	DICLK2	I	VIO1	Tuner audio I^2S, 2 clock
85	DIFS2	I	VIO1	Tuner audio I^2S, 2 frame sync
86	DIN2	I	VIO1	Tuner audio I^2S, 2 data input
87	TTSB0	O	VIO1	Tuner 0 SPI target select, active low
88	TRSTB0	O	VIO1	Tuner 0 reset, active low

3. Package Outline



Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
b	0.20	0.25	0.30
A3		0.203 REF	
D		12.00 BSC	
e		0.5 BSC	
E		12.00 BSC	
D2	6.30	6.40	6.50
E2	6.30	6.40	6.50
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

4. Ordering Guide

4.1. Ordering Part Number Explanation

Si469abccdddAMe

- a = Number of channels supported
  - 2 = two channels
  - 3 = three channels
  - 4 = four channels
- b = Digital Broadcast Standard
  - 1 = HD Radio™
  - 2 = DAB/DAB+
  - 3 = CDR
  - 4 = DRM (DRM for AM, DRM for FM)
- cc = Revision
  - A0 = current revision
- ddd = Device designator
  - GE1 = general device, no customer-programmable MCU
  - GC1 = general device, with customer-programmable MCU
- e = Outer packaging
  - R = Tape and Reel
  - Blank = Tray