DATA SHEET

Si53258/Si53254 8/4-Output PCIe Gen 1/2/3/4/5/6 Clock Buffers

The Si53258/54 are the industry's highest performance and lowest power automotive grade PCI Express fanout buffers for PCIe Gen1/2/3/4/5/6 common clock and/or SRIS applications. The Si53258 and Si53254 source eight and four 100 MHz PCIe differential clock outputs, respectively. All clock outputs are compliant to PCIe Gen1/2/3/4/5/6 common clock and separate reference clock architecture specifications.

Hardware control pins are available for enabling and disabling the outputs, as well as input selection for devices that include dual-input functionality.

For more information about PCI Express, Skyworks' complete PCIe portfolio, application notes, and design tools including Skyworks' PCIe Clock Jitter Tool for PCI Express compliance, visit the Skyworks Timing PCI Express Learning Center page.

Applications

- Infotainment
- ADAS ECU
- Radar sensors
- LiDar sensors

Features

- 8/4-outputs with internal termination
- PCIe Gen 1/2/3/4/5/6 compliant
- AEC-Q100 qualified
- AEC-Q006 qualified
- Automotive Grade 2: –40 to +105 °C
- Internal 100 Ω or 85 Ω line matching
- Excellent additive jitter performance
  - 0.05 ps RMS (Gen 3/4)
  - 0.025 ps RMS (Gen 5)
  - 0.013 ps RMS (Gen 6)
- Spread spectrum tolerant to pass through a spread input clock for EMI reduction
- Individual hardware control pins for Output Enable
- Optional dual input capability with MUX
- 1.8 to 3.3 V power supply
- Pb-free, RoHS-6 compliant

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Features

- 8/4-HCSL outputs with internal termination
- PCIe Gen1/2/3/4/5/6 compliant
- Automotive Grade 2: –40 to +105 °C
- Internal 100 Ω or 85 Ω line matching
- Excellent additive jitter performance
  - 0.05 ps RMS (Gen 3/4)
  - 0.025 ps RMS (Gen 5)
  - 0.013 ps RMS (Gen 6)
- Spread spectrum tolerant to pass through a spread input clock for EMI reduction
- Loss of Signal (LOS) output pin
- Individual hardware control pins for Output Enable
- Optional dual input capability with MUX
- 1.8 to 3.3 V power supply
- Pb-free, RoHS-6 compliant

2. Ordering Guide

Table 1. Si53258/Si53254 Ordering Guide

Number of Outputs	Number of Inputs	Part Number	Package Type	Temperature
8	1	Si53258A-D01AM	40-QFN	Automotive temperature range: –40 to 105 °C
		Si53258A-D01AMR	40-QFN, tape and reel	
	2	Si53258A-D03AM	40-QFN	
		Si53258A-D03AMR	40-QFN, tape and reel	
4	1	Si53254A-D01AM	32-QFN	
		Si53254A-D01AMR	32-QFN, tape and reel	
	2	Si53254A-D03AM	40-QFN	
		Si53254A-D03AMR	40-QFN, tape and reel	

3. Functional Description

3.1. Functional Block Diagrams

3.1.1. Si53258A-D01AM Functional Block Diagram

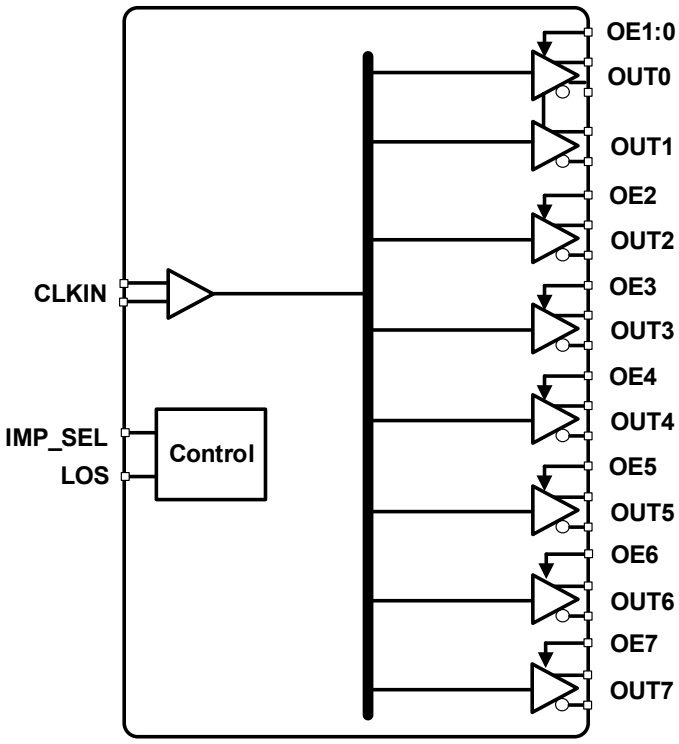


Figure 1. Si53258A-D01AM Functional Block Diagram

3.1.2. Si53254A-D01AM Functional Block Diagram

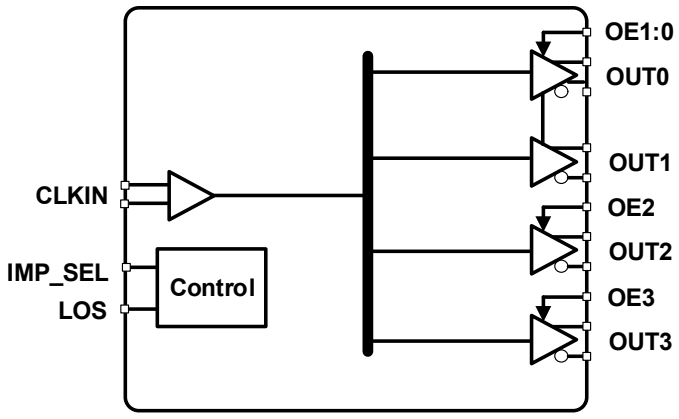


Figure 2. Si53254A-D01AM Functional Block Diagram

3.1.3. Si53258A-D03AM Functional Block Diagram

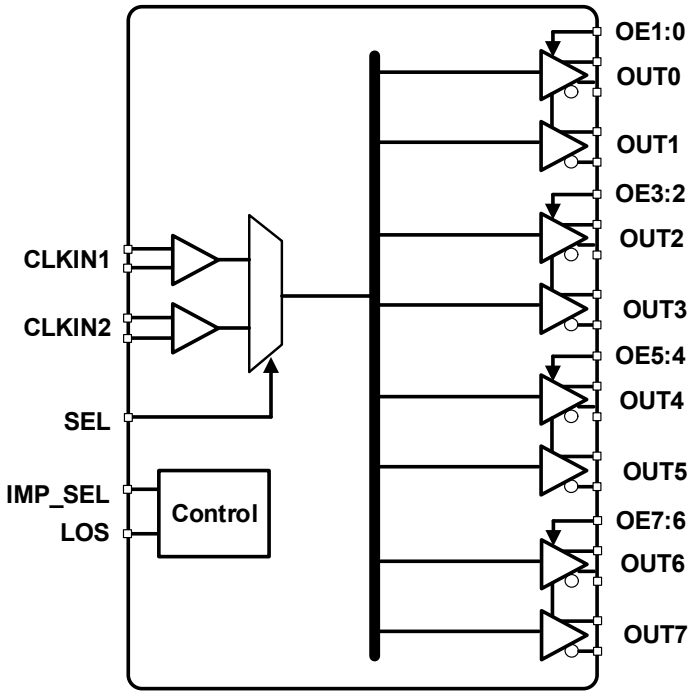


Figure 3. Si53258A-D03AM Functional Block Diagram

3.1.4. Si53254A-D03AM Functional Block Diagram

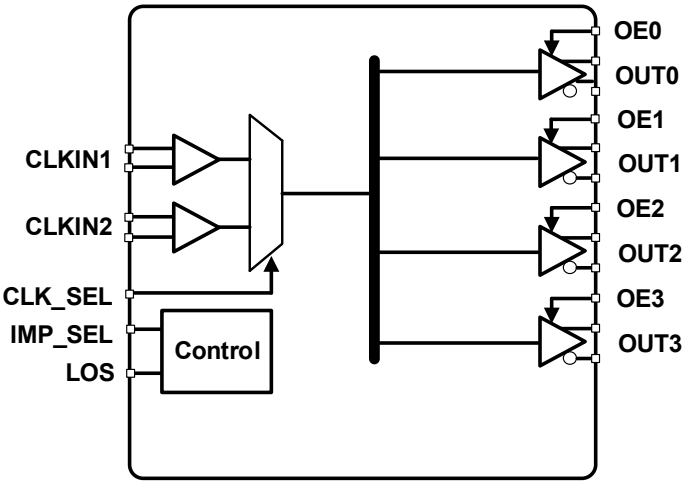


Figure 4. Si53254A-D03AM Functional Block Diagram

3.2. Input Clock Termination

When supplying a differential input clock, ac or dc coupling can be used. The figures below show the ac- and dc-coupled differential input clock connection to the clock input pins. The input clock Format Termination shown in the figures below is dependent on the driver's termination requirements. The Si5325x clock inputs are high-impedance inputs, and the clock driven in must meet the specified electrical requirements.

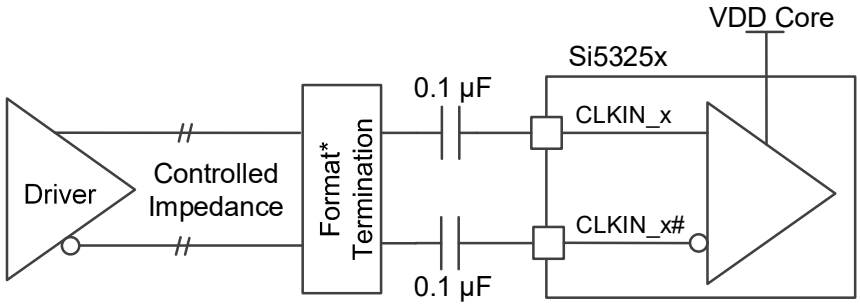


Figure 5. AC-Coupled Differential Input Clock (LVDS, LVPECL, HCSL, CML, etc.)

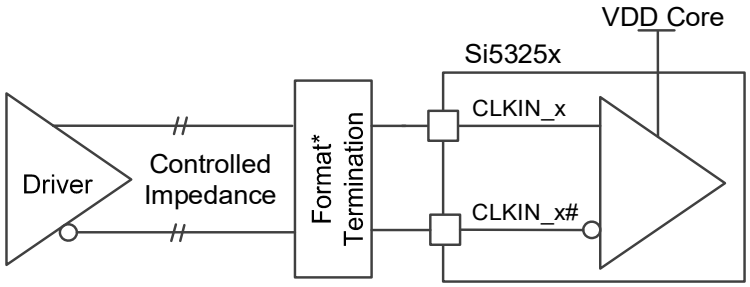


Figure 6. DC-Coupled Differential Input Clock

To determine if a specific dc-coupled differential input clock arrangement is supported, refer to Table 2.

Table 2. Si5325x Input Clock Coupling Restrictions (AC or DC)[1,2]

Format	VDD_Core		
	3.3 V	2.5 V	1.8 V
LVDS 3.3 V/2.5 V	AC or DC	AC only	AC only
LVDS 1.8 V	AC or DC	AC only	AC only
LVPECL 3.3 V/2.5 V	AC or DC	AC only	AC only
HCSL	AC or DC	AC or DC	AC only
CML	AC only	AC only	AC only
LVCMOS	DC only	DC only	DC only

1. For dc-coupled, input clock peak voltage must not exceed VDD_Core and minimum voltage must not be below GND.
2. For ac-coupled LVCMOS, peak swing must not exceed VDD_Core.

Figure 7 below shows how to connect single-ended input clocks, such as LVCMOS. The single-ended clock must be connected to the positive CLKIN input as shown below.

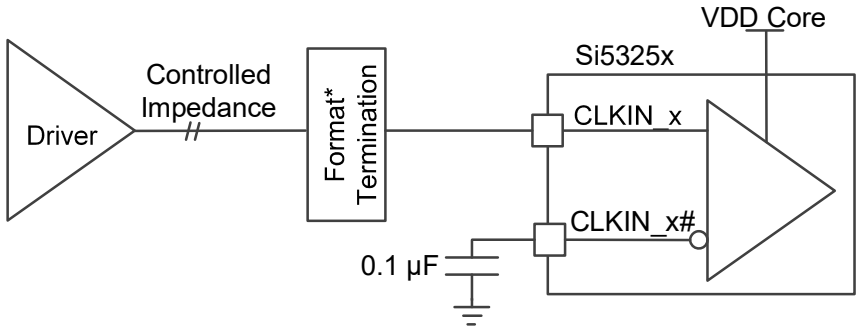


Figure 7. DC-Coupled Single-Ended Input Clock (LVCMOS)

For dc-coupled single-ended input clocks (such as LVCMOS) the Vswing of the clock must be limited to the maximum VDD_Core voltage. (VDD_Core is defined as the following group of VDD supply pins: VDD_DIG, VDDA, and VDD_XTAL.) The Input clock format termination is dependent on the driver format used and is usually specified by the driving device and/or industry standard clock format specification.

For example, in the case of using a LVCMOS input clock, the driving device may recommend a series termination resistor. When using LVCMOS input clocks the Si5325x input must be configured in LVCMOS mode in CBPro. The single-ended CLKIN input of Si5325x is a high impedance input.

3.3. HCSL Differential Output Terminations

3.3.1. Termination for HCSL Outputs

The Si53254/8 HCSL driver features integrated termination resistors to simplify interfacing to an HCSL receiver. The HCSL driver supports both 100 Ω and 85 Ω transmission line options, and can be selected using the IMP_SEL hardware input pin.

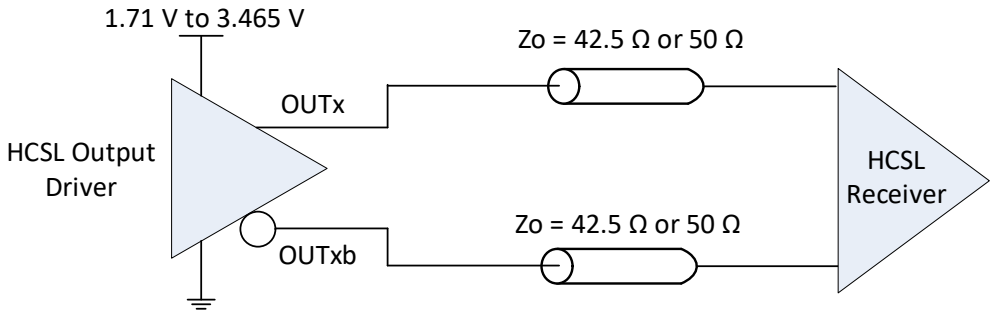


Figure 8. HCSL Internal Termination Mode

3.4. Output Enable/Disable

An output enable pin provides a convenient method of disabling or enabling the output drivers. When the output enable pin is held high, all designated outputs will be disabled. When held low, the designated outputs will be enabled.

3.4.1. For Differential Outputs

Output disabled means the differential output **pair** goes to a logical “0” state. The positive side goes low, and the negative side goes high. The high and low voltage levels are in accordance with the configured output format type for each differential pair. The output pair will statically remain at these levels as long as the output is disabled. Upon being enabled, the outputs will start up synchronous to the output clock to avoid output runt pulses or glitches.

3.5. Loss of Signal (LOS)

The LOS indicator is used to check for the presence of an input reference source (crystal or clock). LOS will assert when the reference source frequency drops below approximately 10 MHz.

The LOS pin must be checked prior to selecting the clock input or should be polled to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin will assume a logic low (LOS = 0) state. When a reference source is present at the associated input clock pin, the LOS pin will assume a logic high (LOS = 1) state.

4. Power Supply Filtering Recommendations

The Si53258/4 features internal LDOs on each power supply pin, providing excellent power supply noise rejection. As a guideline, each power supply pin should use a parallel combination of a 1 µf and a 0.1 µF bypass capacitor placed as close to the supply pin as possible.

5. Electrical Specifications

Table 3. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Units
Storage temperature range	T_{STG}		–55 to +150	°C
DC supply voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	VDD_{xtal}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input voltage range	V_I		–0.3 to 1.3	V
Latch-up tolerance	LU		JESD78 compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction temperature	T_{JCT}		–55 to 125	°C
Soldering temperature	T_{PEAK}		260	°C
Soldering temperature time at T_{PEAK}	T_P		20 to 40	sec

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, visit the Skyworks environmental compliance page.
3. The device is compliant with JEDEC J-STD-020.

Table 4. Recommended Operating Conditions[1]

V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient temperature	T_A		–40	25	105	°C
Junction temperature	TJ_{MAX}		—	—	125	°C
Core supply voltage	V_{DDA}, V_{DD_DIG}, V_{DD}		1.71	—	3.46	V
Output driver supply voltage	V_{DDO}		1.42[2]	—	3.46	V

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.
2. LVCMOS outputs only.

Table 5. DC Characteristics

V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core supply current	I_{DD}			—	11	18	mA
Output buffer supply current	I_{DDOx}	HCSL Output[1] @ 100 MHz		—	20	22	mA
Total power dissipation	P_d	40-pin			530	670	mW
		32-pin		—	145	215	mW

1. Differential outputs terminated into a 100 Ω load at 3.3 V.

Table 6. Clock Input Specifications[1,2]

V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC-Coupled Differential Input Clock on CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#)						
Frequency	F_{IN}	Differential	—	100	—	MHz
Voltage swing	V_{PP_DIFF}[3]		0.5	—	1.8	V_{PP_diff}
Slew rate	SR/SF	20 to 80%	0.75	—	—	V/ns
Duty cycle	DC		40	—	60	%
Input impedance	R_{IN}		10	—	—	kΩ
Input capacitance	C_{IN}		2	3.5	6	pF

1. Imposed for jitter performance.
2. Rise and Fall times may be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.08 – 0.2) \times V_{IN\_Vpp\_se}) / SR$.
3. $V_{PP\_DIFF} = 2 \times V_{PP\_SINGLE\text{-}ENDED}$

Table 7. Control Pins

V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, T_A = –40 to 105 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
OEB_OUTx, IMP_SEL Pins (Inputs)						
Input voltage	V_{IL}		–0.1	—	0.3 x V_{DD}[1]	V
	V_{IH}		0.7 x V_{DD}[1]	—	1.1 x V_{DD}[1]	V
Input capacitance	C_{IN}		—	—	4	pF
Pull-up/down resistance	R_{IN}		—	50	—	kΩ
LOS Pin (Output)						
Output voltage	V_{OL}	Pull-up = 1kΩ	—	—	0.4	V
Pull-up resistance	R_{PU}		1	—	10	kΩ
LOS assertion time			—	120	—	µs
LOS deassertion time			—	95	—	µs

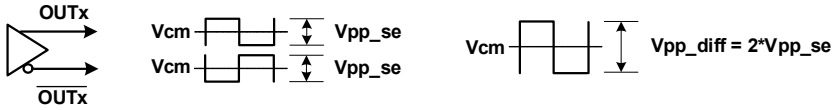
1. VDD indicates all core voltages, VDD_DIG and VDDA, that must use the same nominal voltage.

Table 8. Differential Clock Output Specifications

V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output frequency	f_{OUT}				100		MHz
Duty cycle	DC	With 50% duty cycle input.		48	—	52	%
Output-output skew	T_{SK}			—	—	80	ps
Output voltage swing	V_{SEPP}	HCSL		0.7	0.8	0.9	V_{PP}
Common mode voltage	V_{CM}	HCSL		0.35	0.4	0.45	V
HCSL edge rate	Edgr	Notes 1,2,3		1	—	4.5	V/ns
HCSL delta-tr	D_{tr}	Notes 2,4,5		—	—	155	ps
HCSL delta-tf	D_{tf}	Notes 2,4,5		—	—	155	ps
HCSL Vcross abs	V_{xa}	Notes 2,4,6,7		250	—	550	mV
HCSL delta Vcross	D_{vcrs}	Notes 2,4,8		—	—	140	mV
HCSL V_{ovs}	V_{ovs}	Notes 2,4,9		—	—	V_{HIGH} + 300	mV
HCSL V_{uds}	V_{uds}	Notes 2,4,10		—	—	V_{LOW} – 300	mV
HCSL V_{rng}	V_{rng}	Notes 2,4		V_{HIGH} – 200	—	V_{LOW} + 200	mV
Rise and fall times (20% to 80%)	t_R/t_F	HCSL		—	—	420	ps

1. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from –150 mV to +150 mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for rising clock and falling clock#. Signal must be monotonic through the V_{OL} to V_{OH} region for T_{rise} and T_{fall}.
2. Applies to a 2 pf load with both internal or external 50 Ω or 42.5 Ω Rp.
3. Measurement taken from differential waveform.
4. Measurement taken from single ended waveform.
5. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.



6. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
7. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
8. ΔV_{cross} is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in V_{cross} for any particular system.
9. Overshoot is defined as the absolute value of the maximum voltage.
10. Undershoot is defined as the absolute value of the minimum voltage.

Table 9. Performance Characteristics
V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 105 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power ramp	t_{VDD}	0 V to V_{DDmin}	0.1	—	10	ms
Clock stabilization from power-up	t_{STABLE}	Time for clock outputs to appear after POR	—	15	25	ms

Table 10. PCI-Express Clock Output Additive Phase Jitter (100 MHz)
V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 V to 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Test Condition	Typ	Max	Units
PCIe Gen 1.1	Includes PLL BW 1.5–22 MHz, Peaking = 3 dB, Td = 10 ns, Ftrk = 1.5 MHz with BER = 1E-12[1]	11	19	ps RMS
PCIe Gen 2.1	Includes PLL BW 5MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td=12ns, Low Band, F < 1.5 MHz	0.02	0.026	ps RMS
	Includes PLL BW 5 MHz and 8–16 MHz, Jitter Peaking = 0.01–1 dB and 3 dB, Td = 12 ns, High Band, 1.5 MHz < F < Nyquist[1]	0.2	0.31	ps RMS
PCIe Gen 3.0	Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1 dB, Td = 12 ns, CDR = 10 MHz [1,2]	0.06	0.1	ps RMS
PCIe Gen 4.0	Includes PLL BW 2–4 MHz and 5 MHz, Peaking = 0.01–2 dB and 1dB, Td = 12 ns, CDR = 10 MHz[1,2]	0.05	0.1	ps RMS
PCIe Gen5.0	Includes PLL BW 500 kHz–1.8 MHz, CDR = 20 MHz[1,2]	0.025	0.04	ps RMS
PCIe Gen 6.0	Includes PLL BW 500 kHz–1 MHz, CDR = 20 MHz[1,2]	0.013	0.017	ps RMS

1. All output clocks 100 MHz HCSL format. Jitter data taken from clock jitter tool.
2. Excludes oscilloscope sampling noise.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Units
40 QFN				
Thermal resistance, junction-to-ambient	θ_{JA}	Still air	23.1	°C/W
		Air flow 1 m/s	17.5	
		Air flow 2 m/s	16.5	
Thermal resistance, junction-to-case	θ_{JC}		13.4	
Thermal resistance, junction-to-board	θ_{JB}		8.7	
	ψ_{JB}		8.4	
32 QFN				
Thermal resistance, junction-to-ambient	θ_{JA}	Still air	28.4	°C/W
		Air flow 1 m/s	24	
		Air flow 2 m/s	23	
Thermal resistance, junction-to-case	θ_{JC}		15.9	
Thermal resistance, junction-to-board	θ_{JB}		11.5	
	ψ_{JB}		11.2	

1. Based on JEDEC standard 4-layer PCB.

6. Pin Descriptions

6.1. Si53258A-D01AM Pin Descriptions (40-QFN)

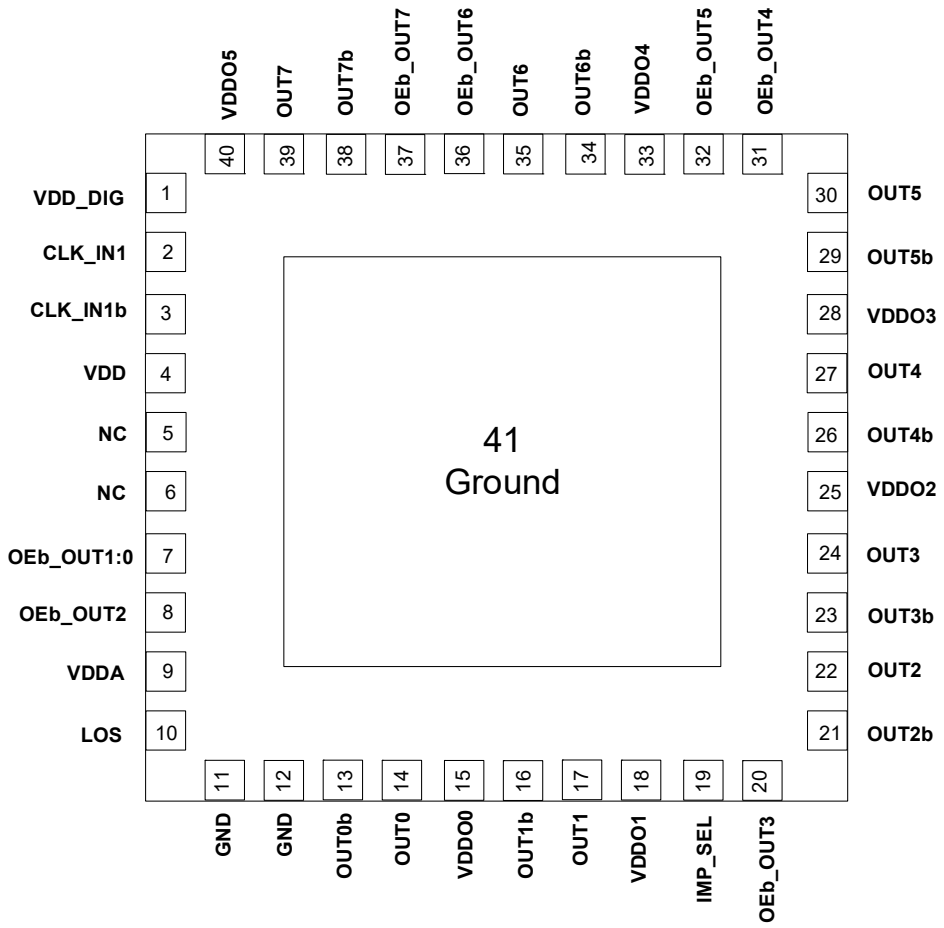


Figure 9. Si53258A-D01AM 40-QFN

Table 12. Si53258A-D01AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	**Voltage supply for digital functions** Connect to 1.8 to 3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLK_IN1	I	**100 MHz HCSL Clock1 input** These pins are high-impedance and must be terminated externally.
3	CLK_IN1b	I	
4	VDD	P	**Voltage supply** Connect to 1.8 to 3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.

Table 12. Si53258A-D01AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
5	NC	I	No Connect. Do not connect these pins to anything.
6	NC	I	
7	OEb_OUT1:0	I	**Output enable pin for OUT1 and OUT0** Low = output enabled High = output disabled
8	OEb_OUT2	I	**Output enable pin for OUT2** Low = output enabled High = output disabled
9	VDDA	P	**Core supply voltage** Connect to 1.8 to 3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
10	LOS	O	The LOS status pin indicates whether the reference input has dropped below approximately 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected. 0 = reference input has dropped below approx. 10 MHz 1 = reference input is present (>10 MHz)
11	GND	P	Connect these pins to ground.
12	GND	P	
13	OUT0b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
14	OUT0	O	
15	VDDO0	P	**Supply voltage (1.8 to 3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
17	OUT1	O	
18	VDDO1	P	**Supply voltage (1.8 to 3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	IMP_SEL	I	**Impedance select pin for output drivers** IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω

Table 12. Si53258A-D01AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
20	OEb_OUT3	I	**Output enable pin for OUT3** Low = output enabled High = output disabled
21	OUT2b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
22	OUT2	O	
23	OUT3b	O	**Output clock** Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
24	OUT3	O	
25	VDDO2	P	**Supply voltage (1.8 to 3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
27	OUT4	O	
28	VDDO3	P	**Supply voltage (1.8 to 3.3 V) for OUT4 and OUT5** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
30	OUT5	O	
31	OEb_OUT4	I	**Output enable pin for OUT4** Low = output enabled High = output disabled
32	OEb_OUT5	I	**Output enable pin for OUT5** Low = output enabled High = output disabled
33	VDDO4	P	**Supply voltage (1.8 to 3.3 V) for OUT6** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
35	OUT6	O	
36	OEb_OUT6	I	**Output enable pin for OUT6** Low = output enabled High = output disabled

Table 12. Si53258A-D01AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
37	OEb_OUT7	I	**Output enable pin for OUT7** Low = output enabled High = output disabled
38	OUT7b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
39	OUT7	O	
40	VDDO5	P	**Supply voltage (1.8 to 3.3 V) for OUT7** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	GND PAD	P	**Ground pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.2. Si53258A-D03AM Pin Descriptions (40-QFN)

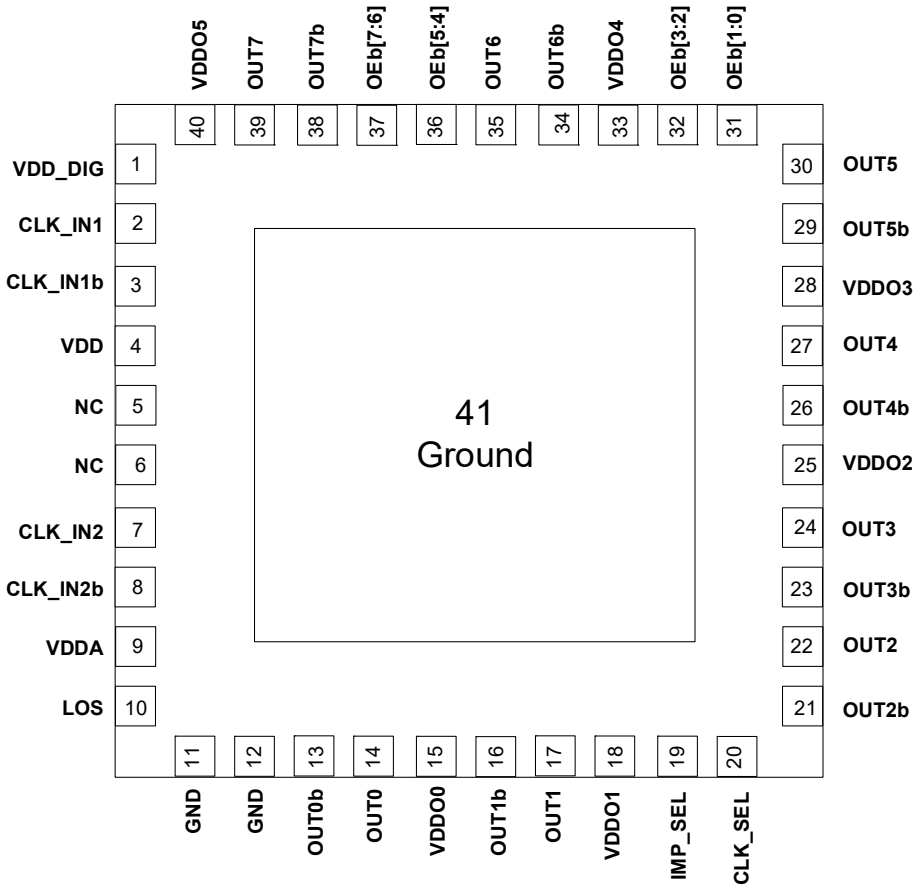


Figure 10. Si53258A-D03AM 40-QFN

Table 13. Si53258A-D03AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8 to 3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA.
2	CLK_IN1	I	**100 MHz HCSL Clock1 input** These pins are high-impedance and must be terminated externally. If both the CLK_IN1 and CLK_IN1b inputs are unused and deselected, then both inputs can be left floating.
3	CLK_IN1b	I	
4	VDD	P	**Voltage supply** Connect to 1.8 to 3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	I	**No connect** Do not connect these pins to anything.
6	NC	I	
7	CLK_IN2	I	**100 MHz HCSL Clock2 input** These pins are high-impedance and must be terminated externally. If both the CLK_IN2 and CLK_IN2b inputs are unused and deselected, then both inputs can be left floating.
8	CLK_IN2b	I	

Table 13. Si53258A-D03AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
9	VDDA	P	**Core supply voltage** Connect to 1.8 to 3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
10	LOS	O	The LOS status pin indicates whether the reference input has dropped below approximately 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected. 0 = reference input has dropped below approx. 10 MHz 1 = reference input is present (>10 MHz)
11	GND	P	Connect this pin to ground.
12	GND	P	Connect this pin to ground.
13	OUT0b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
14	OUT0	O	
15	VDDO0	P	**Supply voltage (1.8 to 3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
17	OUT1	O	
18	VDDO1	P	**Supply voltage (1.8 to 3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	IMP_SEL	I	**Impedance select pin for output drivers** IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω
20	CLK_SEL	I	**Input clock select** Low = CLK_IN1 High = CLK_IN2
21	OUT2b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
22	OUT2	O	
23	OUT3b	O	**Output clock** Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
24	OUT3	O	
25	VDDO2	P	**Supply voltage (1.8 to 3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.

Table 13. Si53258A-D03AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
26	OUT4b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
27	OUT4	O	
28	VDDO3	P	**Supply voltage (1.8 to 3.3 V) for OUT4 and OUT5** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
30	OUT5	O	
31	OEb[1:0]	I	**Output enable pin for OUT1 and OUT0** Low = output enabled High = output disabled
32	OEb[3:2]	I	**Output enable pin for OUT2 and OUT3** Low = output enabled High = output disabled
33	VDDO4	P	**Supply voltage (1.8 to 3.3 V) for OUT6** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
35	OUT6	O	
36	OEb[5:4]	I	**Output enable pin for OUT1 and OUT0** Low = output enabled High = output disabled
37	OEb[7:6]	I	**Output enable pin for OUT6 and OUT7** Low = output enabled High = output disabled
38	OUT7b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
39	OUT7	O	
40	VDDO5	P	**Supply voltage (1.8 to 3.3 V) for OUT7** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	GND PAD	P	**Ground pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.3. Si53254A-D01AM Pin Descriptions (32-QFN)

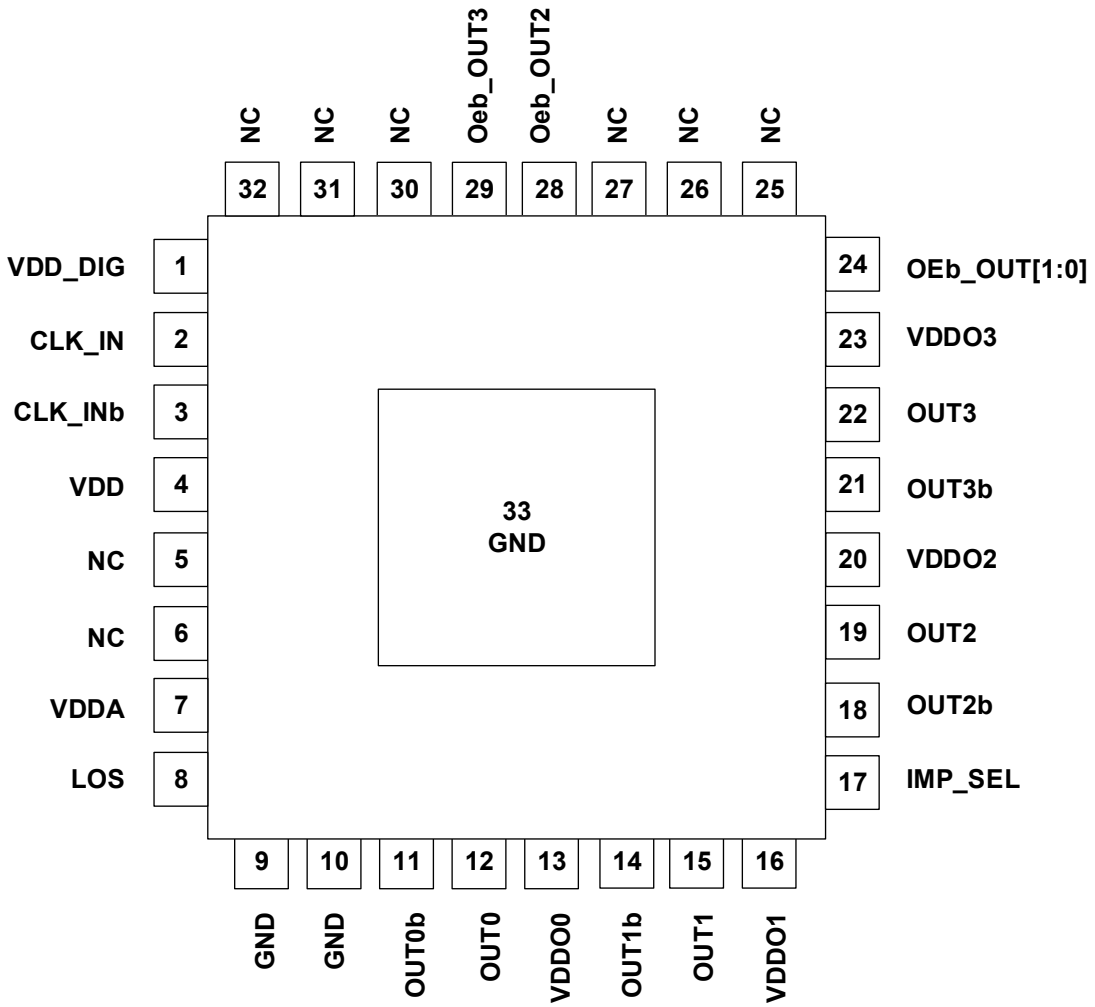


Figure 11. Si53254A-D01AM 32-QFN

Table 14. Si53254A-D01AM Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	**Voltage supply for digital functions** Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLK_IN	I	**100 MHz HCSL clock input** These pins are high-impedance and must be terminated externally.
3	CLK_INb	I	
4	VDD		**Voltage supply** Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.

Table 14. Si53254A-D01AM Pin Descriptions, (32-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
5	NC	—	Do not connect these pins to anything.
6	NC	—	
7	VDDA	P	**Core supply voltage** Connect to 1.8 to 3.3 V. See the Si5332-AM1/2/3 Automotive Grade Device Reference Manual for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD.
8	LOS	O	The LOS status pin indicates whether the reference clock input is above 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected. 0 = reference input has dropped below 10 MHz 1 = reference present (>10 MHz)
9	GND	P	Connect these pins to ground.
10	GND	P	
11	OUT0b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
12	OUT0	O	
13	VDDO0	P	**Supply voltage (1.8 to 3.3 V) for OUT0** See the Si5332-AM1/2/3 Automotive Grade Device Reference Manual for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT1b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
15	OUT1	O	
16	VDDO1	P	**Supply voltage (1.8 to 3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	IMP_SEL	I	**Impedance select pin for output drivers** IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω
18	OUT2b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
19	OUT2	O	
20	VDDO2	P	**Supply voltage (1.8 to 3.3 V) for OUT2** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.

Table 14. Si53254A-D01AM Pin Descriptions, (32-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
21	OUT3b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
22	OUT3	O	
23	VDDO3	P	**Supply voltage (1.8–3.3 V) for OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
24	OEb_OUT[1:0]	I	**Output enable for OUT1 and OUT0** Low = output enabled High = output disabled
25	NC	—	**No connect** Do not connect these pins to anything.
26	NC	—	
27	NC	—	
28	OEb_OUT2	I	**Output enable for OUT2** Low = output enabled High = output disabled
29	OEb_OUT3	I	**Output enable for OUT3** Low = output enabled High = output disabled
30	NC	—	**No connect** Do not connect these pins to anything.
31	NC	—	
32	NC	—	
33	GND PAD	P	**Ground pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

6.4. Si53254A-D03AM Pin Descriptions (40-QFN)

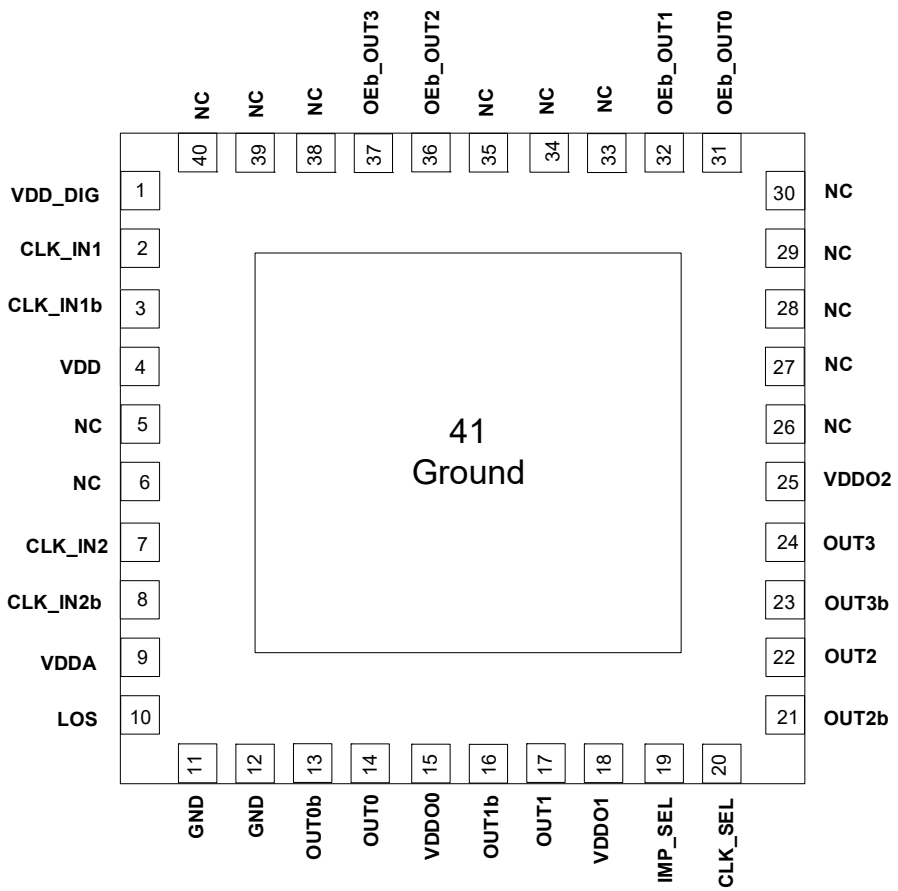


Figure 12. Si53254A-D03AM 40-QFN

Table 15. Si53254A-D03AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8 to 3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLK_IN	I	100 MHz HCSL clock input. These pins are high-impedance and must be terminated externally.
3	CLK_INb	I	
4	VDD	P	**Voltage supply** Connect to 1.8 to 3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA.
5	NC	I	Do not connect these pins to anything.
6	NC	I	
7	CLK_IN2	I	100 MHz HCSL clock input. These pins are high-impedance and terminated externally.
8	CLK_IN2b	I	

Table 15. Si53254A-D03AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
9	VDDA	P	**Core supply voltage** Connect to 1.8 to 3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
10	LOS	O	The LOS status pin indicates if the reference clock input is above 10 MHz. LOS is active low, open drain output and requires an external pull-up resistor of 1 to 10 kΩ for proper operation. If LOS is not required, this pin can be left unconnected. 0 = reference input has dropped below 10 MHz 1 = reference present (>10 MHz)
11	GND	P	Connect these pins to ground.
12	GND	P	
13	OUT0b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
14	OUT0	O	
15	VDDO0	P	**Supply voltage (1.8 to 3.3 V) for OUT0** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
17	OUT1	O	
18	VDDO1	P	**Supply voltage (1.8 to 3.3 V) for OUT1** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	IMP_SEL	I	**Impedance select pin for output drivers** IMP_SEL pin is sampled at power-up only. Low = 100 Ω High = 85 Ω
20	CLK_SEL	I	**Input clock select** Low = CLK_IN1 High = CLK_IN2
21	OUT2b	O	**Output clock** 100 MHz HCSL output. Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
22	OUT2	O	
23	OUT3b	O	**Output clock** Termination recommendations are provided in "3.3. HCSL Differential Output Terminations" on page 8. Unused outputs should be left unconnected.
24	OUT3	O	

Table 15. Si53254A-D03AM Pin Descriptions (40-QFN) (Continued)

Pin Number	Pin Name	Pin Type	Function
25	VDDO2	P	**Supply voltage (1.8 to 3.3 V) for OUT2 and OUT3** Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	NC	—	**No connect** Do not connect these pins to anything.
27	NC	—	
28	NC	—	
29	NC	—	
30	NC	—	
31	OEb_OUT0	I	**Output enable pin for OUT0** Low = output enabled High = output disabled
32	OEb_OUT1	I	**Output enable pin for OUT1** Low = output enabled High = output disabled
33	NC	—	**No Connect** Do not connect these pins to anything.
34	NC	—	
35	NC	—	
36	OEb_OUT2	I	**Output enable pin for OUT2** Low = output enabled High = output disabled
37	OEb_OUT3	I	**Output enable pin for OUT3** Low = output enabled High = output disabled
38	NC	—	**No connect** Do not connect these pins to anything.
39	NC	—	
40	NC	—	
41	GND PAD	P	**Ground pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

7. Package Outline

7.1. 6x6 mm 40-QFN Package Diagram

The figure below illustrates the package details for 40-QFN. The table below lists the values for the dimensions shown in the illustration.

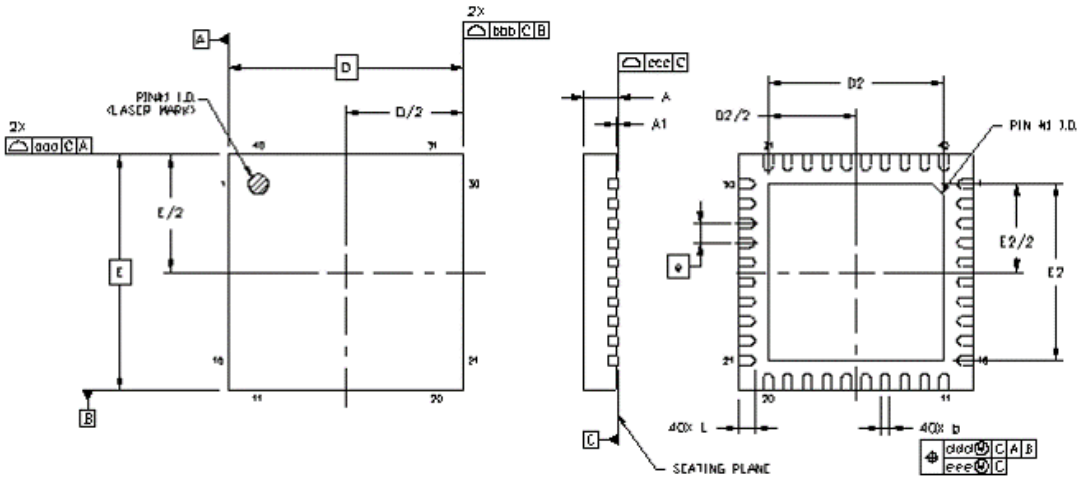


Figure 13. 40-Pin Quad Flat No-Lead (QFN)

Table 16. Package Dimensions[1,2,3,4]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee			0.05

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2. 5x5 mm 32-QFN Package Diagram

Figure 14 illustrates the package details for 32-QFN option. Table 17 lists the values for the dimensions shown in the illustration.

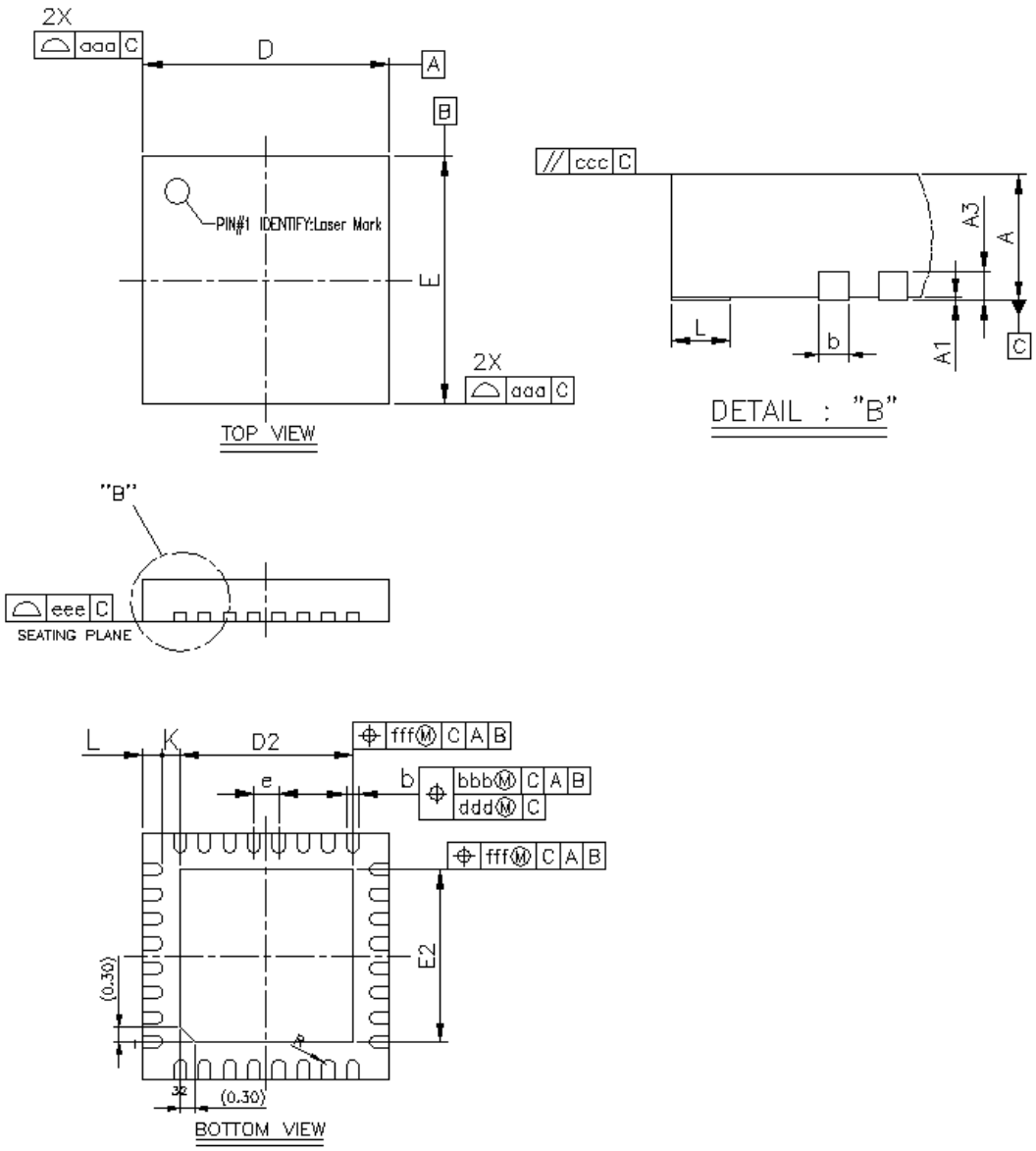


Figure 14. 32-Pin Quad Flat No-Lead (QFN)

Table 17. Package Dimensions[1,2,3,4]

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.09	---	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

8.1. 40-QFN Land Pattern

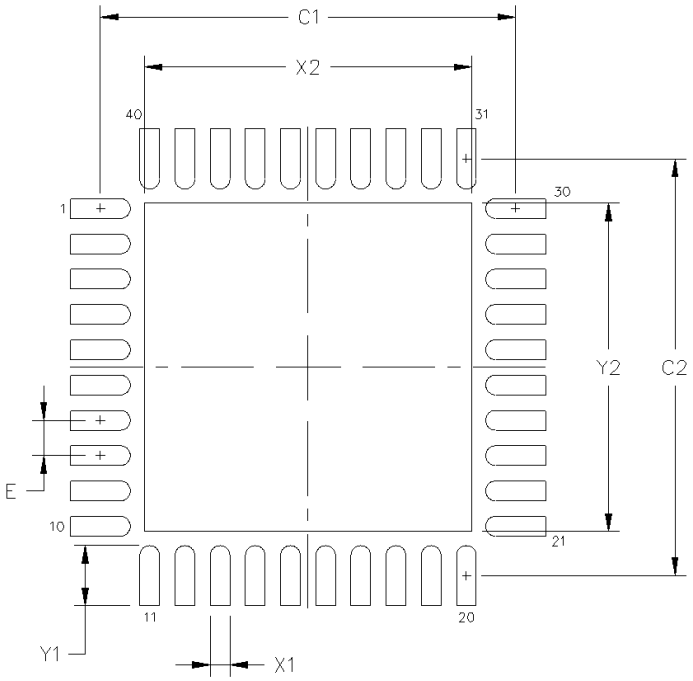


Figure 15. 40-QFN Land Pattern

Table 18. PCB Land Pattern Dimensions

Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3×3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
Card Assembly
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2. 32-QFN Land Pattern

Figure 16 illustrates the PCB land pattern details for 32-QFN package. Table 19 lists the values for the dimensions shown in the illustration.

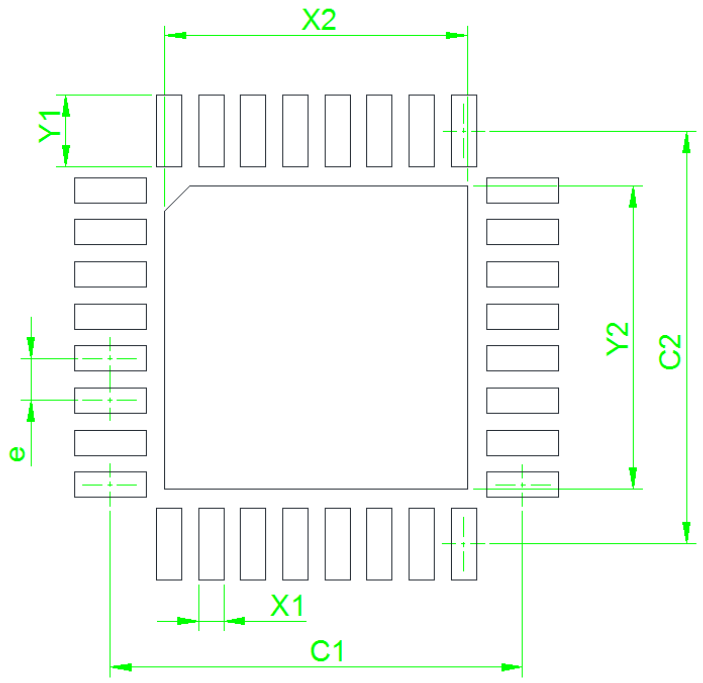


Figure 16. 32-QFN Land Pattern

Table 19. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Notes:
General
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3×3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.

Card Assembly
1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

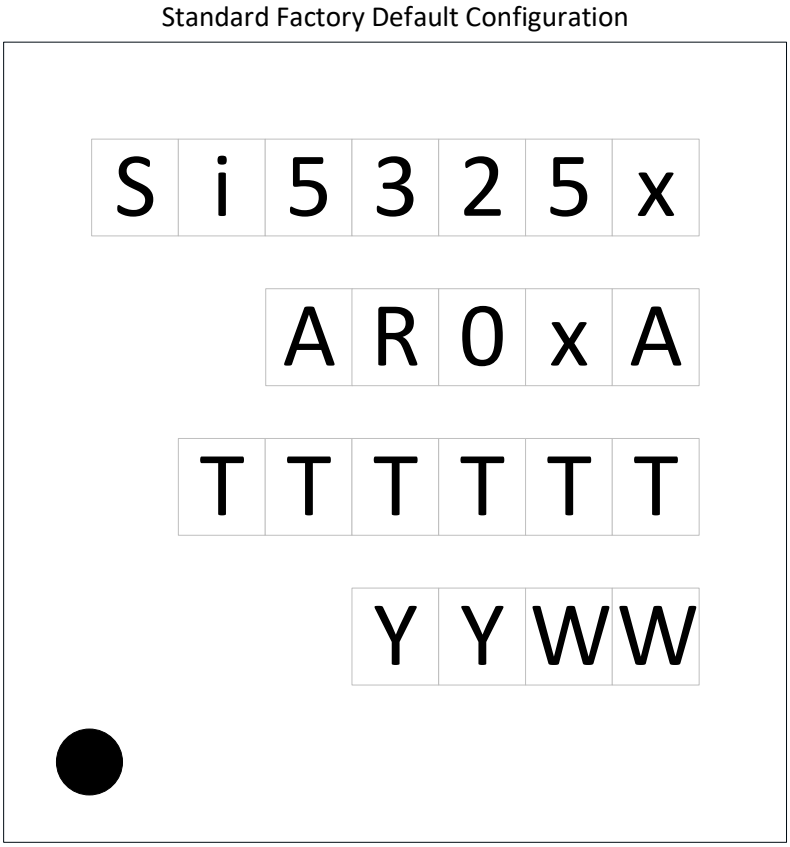


Figure 17. Top Marking

Table 20. Top Marking Explanation

Line	Characters	Description
1	Si53258 Si53254	Base part number
2	A-D0xA	A = Grade R = Product revision (reference ordering section for latest revision) 0x = Product identification, single input: 01 = Single input 03 = Dual input A = Automotive grade temperature range
3	TTTTTT	Manufacturing trace code
4	YYWW	Year (YY) and work week (WW) of package assembly

10. Revision History

Revision	Date	Description	Notes
B	December, 2023	• Added PCIe Gen 6.0 references to front page and "1. Features" on page 2. • Updated Ordering Guide Si53258 and Si53254 "D02" part numbers to "D03". • Updated Table 10, "PCI-Express Clock Output Additive Phase Jitter (100 MHz)," on page 13. - Added PCIe Gen 6.0 specs.	CN0117826
A	July, 2022	• Added Agile data sheet revision in footer.	
1.0	January, 2021	• Updated notes in Table 8, "Differential Clock Output Specifications," on page 12. • Removed "default low" from OEb pin descriptions.	CN0098301
0.7	September, 2022	Initial release.	CN0096966